Fakultät für
Informatik und
Mathematik

HOCHSCHULE
FÜR ANGEWANDTE
WISSENSCHAFTEN
MÜNCHEN

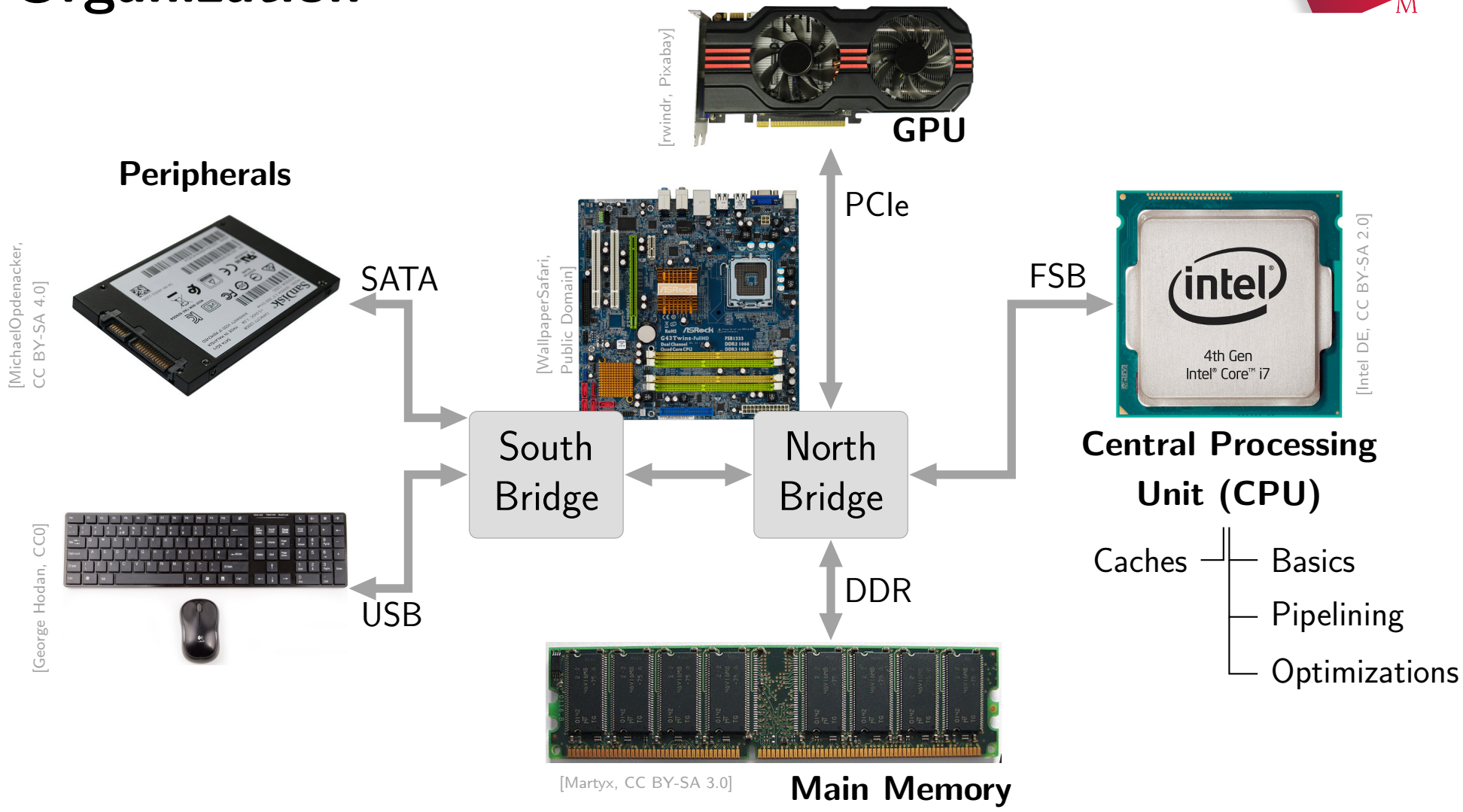
COMPUTER ARCHITECTURE

Chapter 2 – CPU Basics

Prof. Dr.-Ing. Stefan Wallentowitz

Department 07 – Munich University of Applied Sciences

Course Organization



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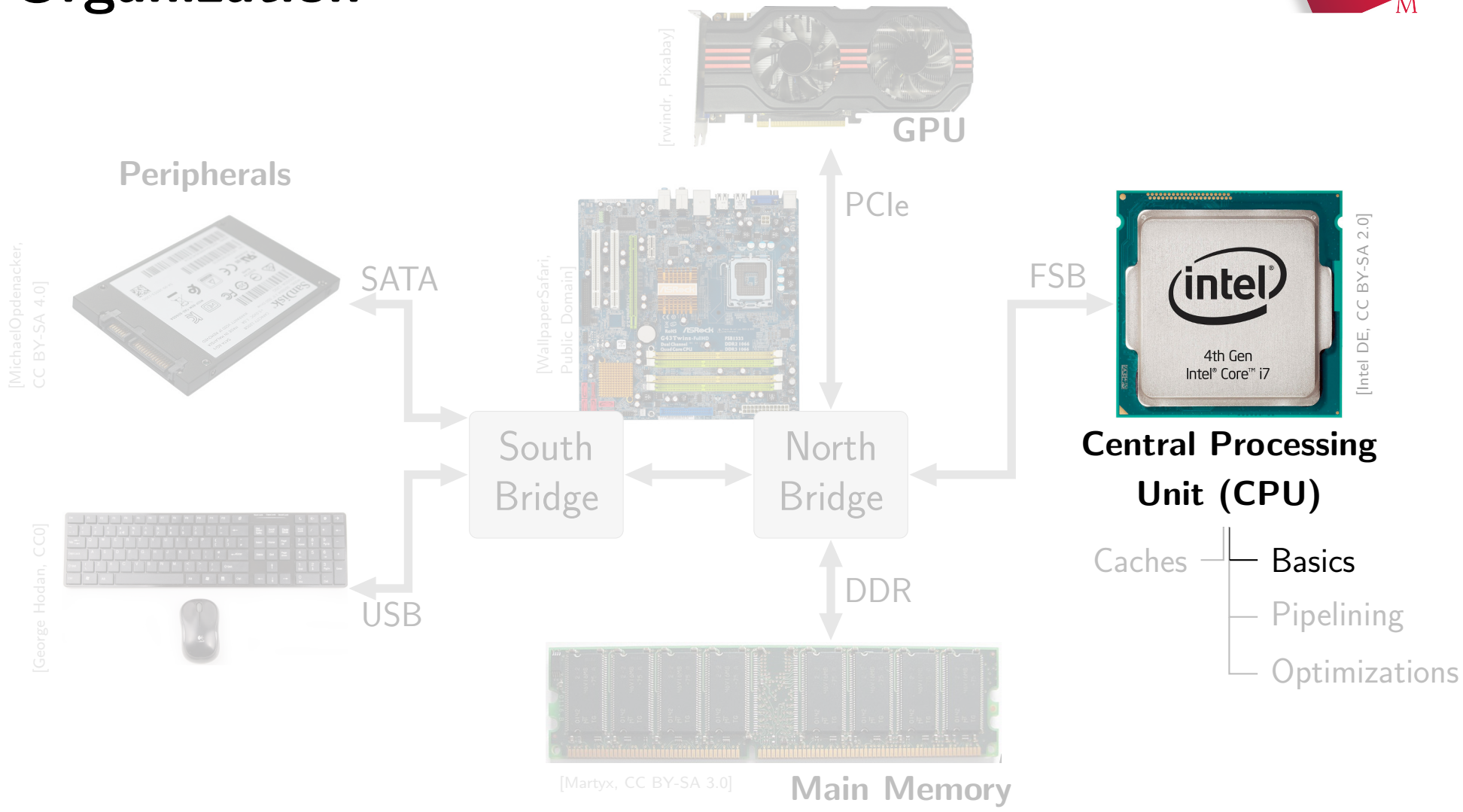

Learning Objectives

- Understand the role of the instruction set architecture

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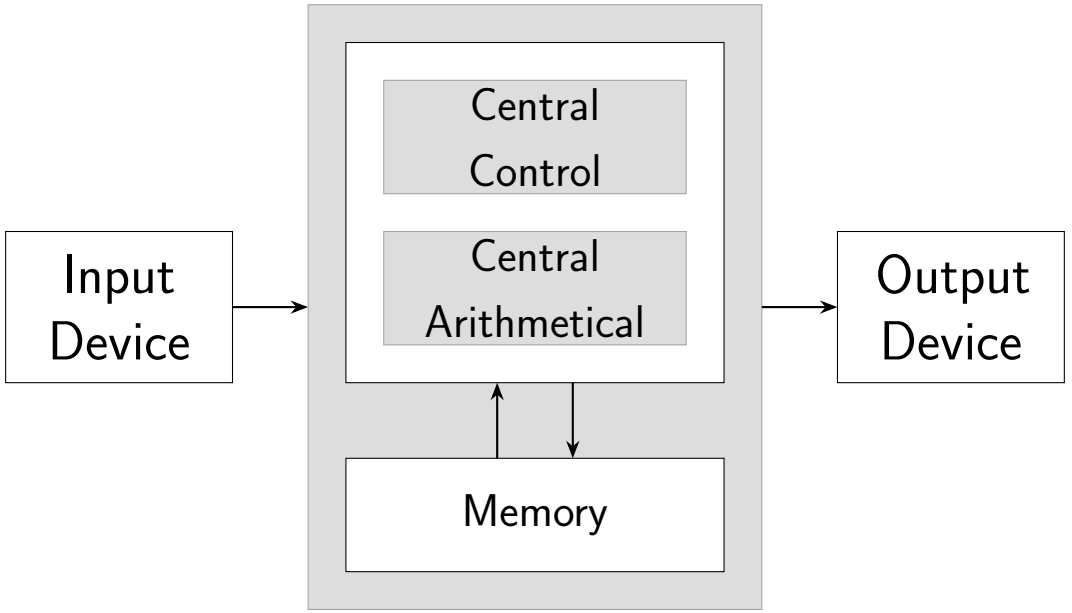
- Understand the role of the instruction set architecture
- Design programs in assembly/machine code from an instruction set architecture
- Apply rules and definition from an instruction set architecture in software development
- Understand the general principle and draw conclusions from it for practical tasks

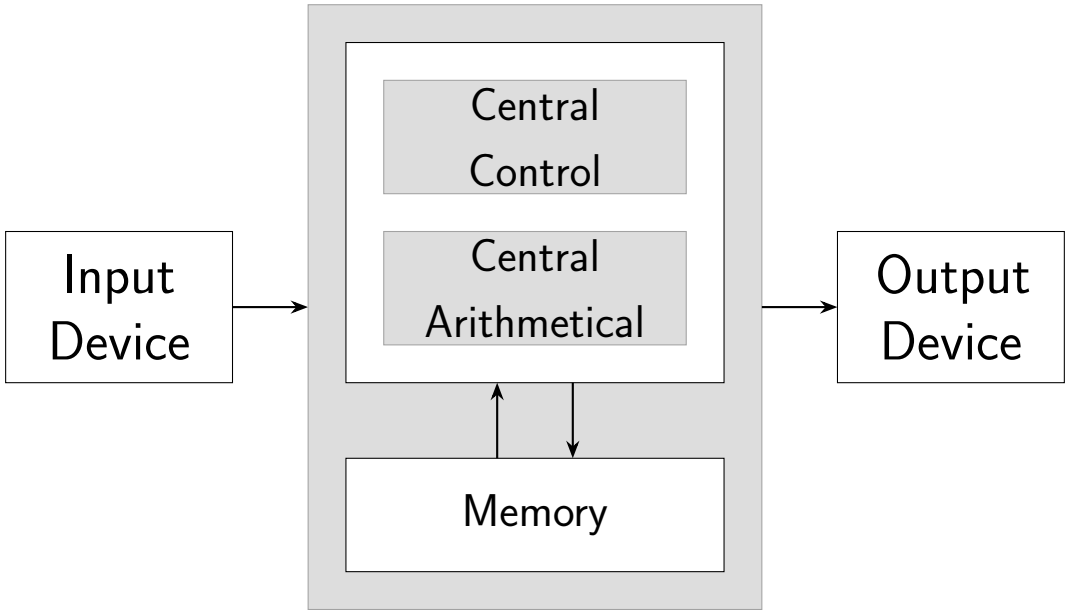
Von Neumann Architecture

- Description of generic computer



Von Neumann Architecture

- Description of generic computer
- Computer organization independent of problem



Von Neumann Architecture

- Description of generic computer
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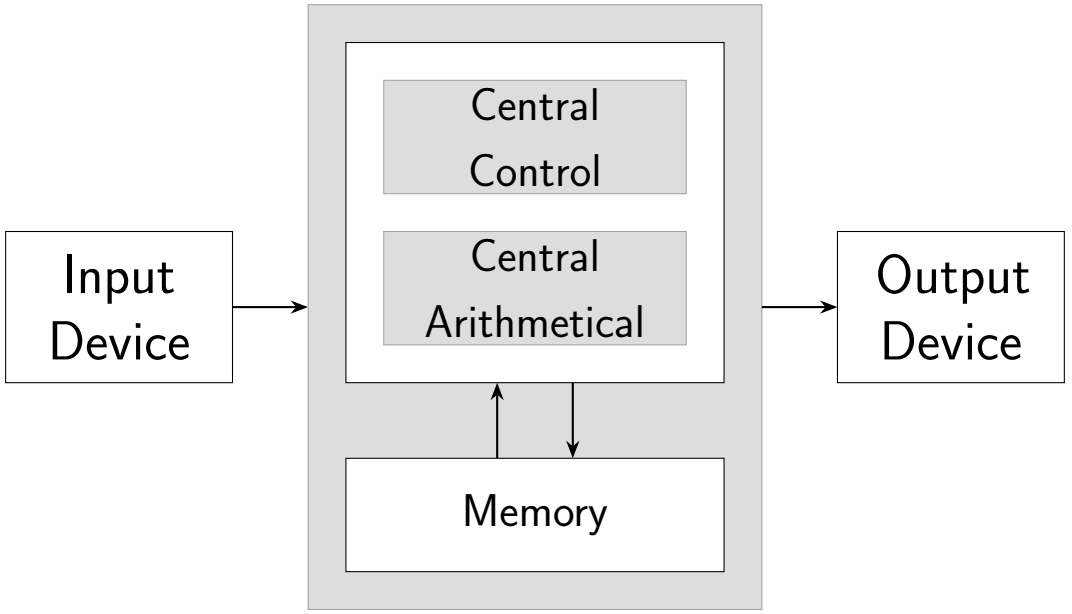

Von Neumann Architecture

- Description of generic computer
- Computer organization independent of problem
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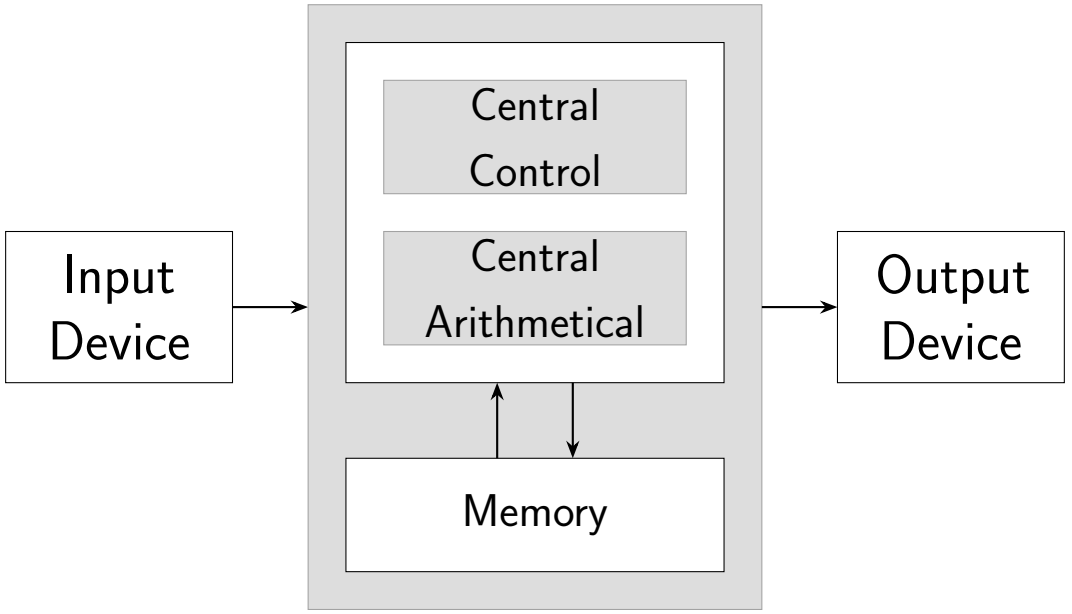
  - Intermediate results



Von Neumann Architecture

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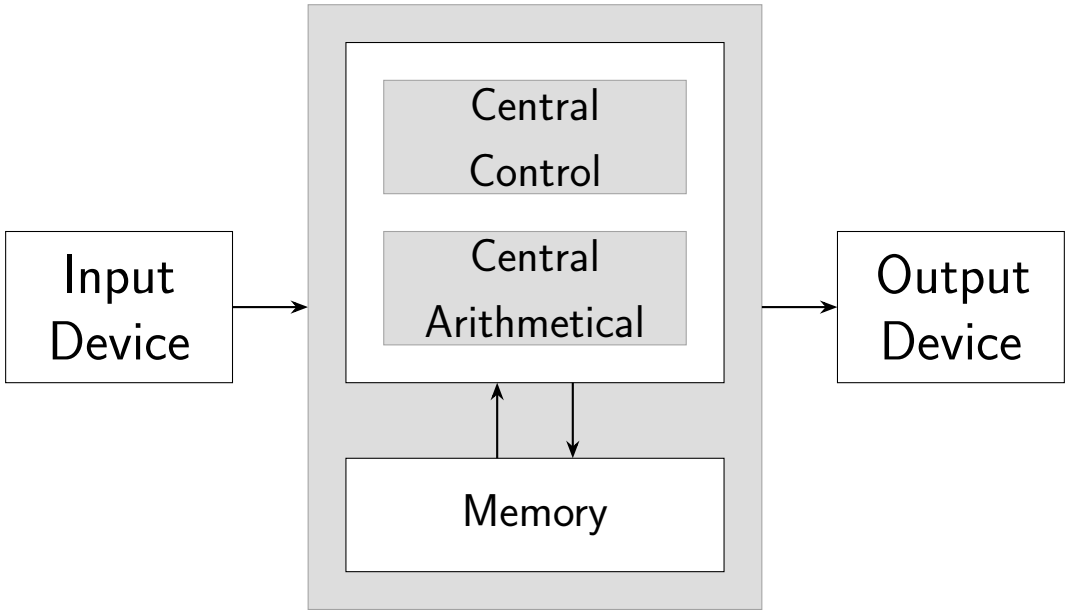

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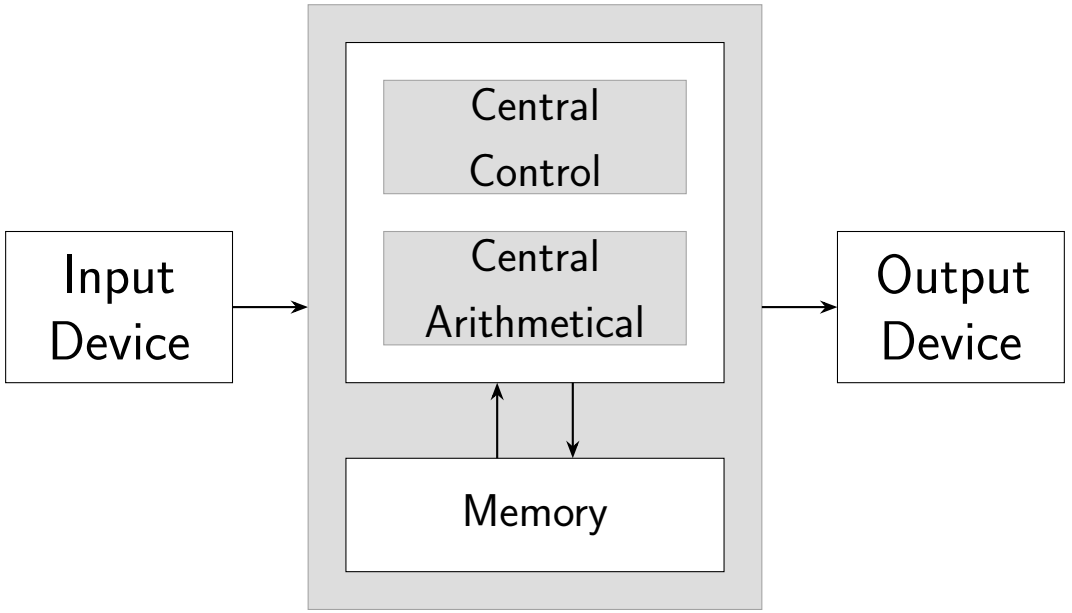

Von Neumann Architecture

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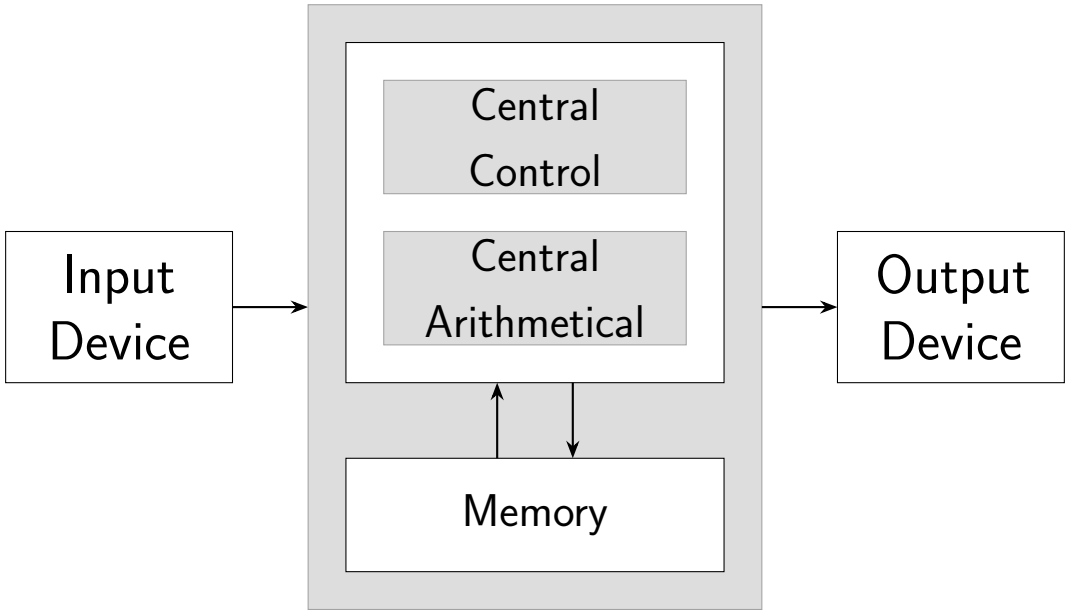
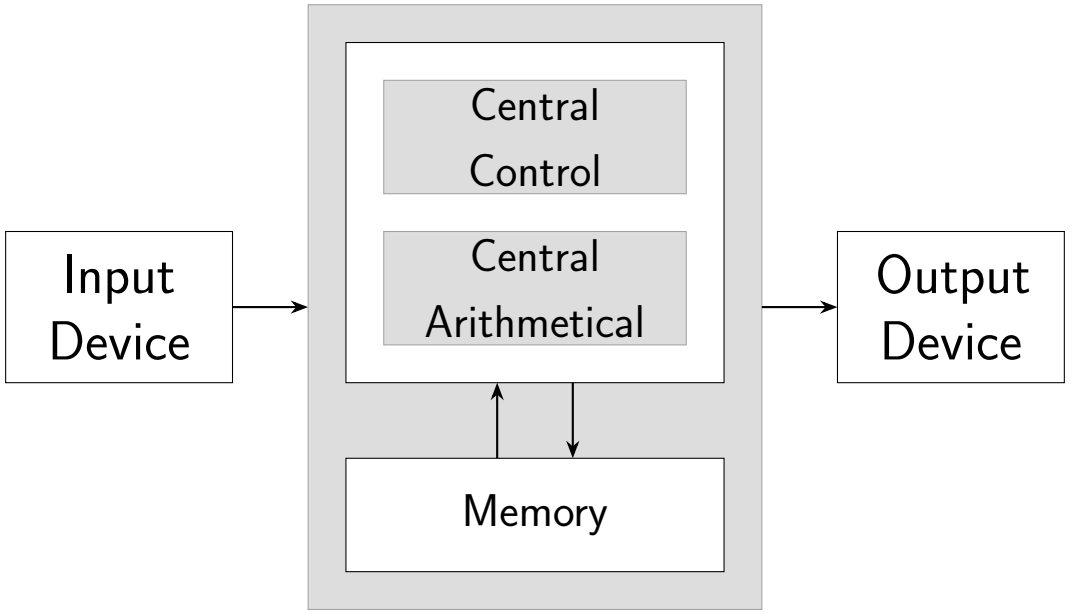


Von Neumann Architecture

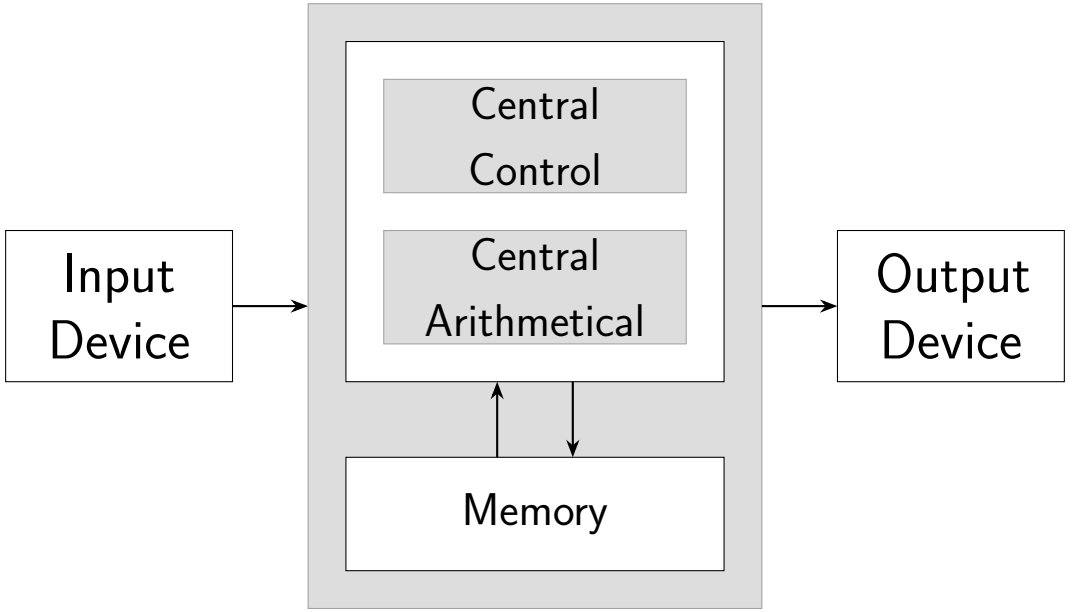
- Description of generic computer
- Computer organization independent of problem
- Memory
  - Intermediate results
  - Stored programs
  - Organized in homogeneous cells
  - Linearly addressed (data and program)
- Program counter in "central control" points to next instruction



Von Neumann Architecture

Control Flow

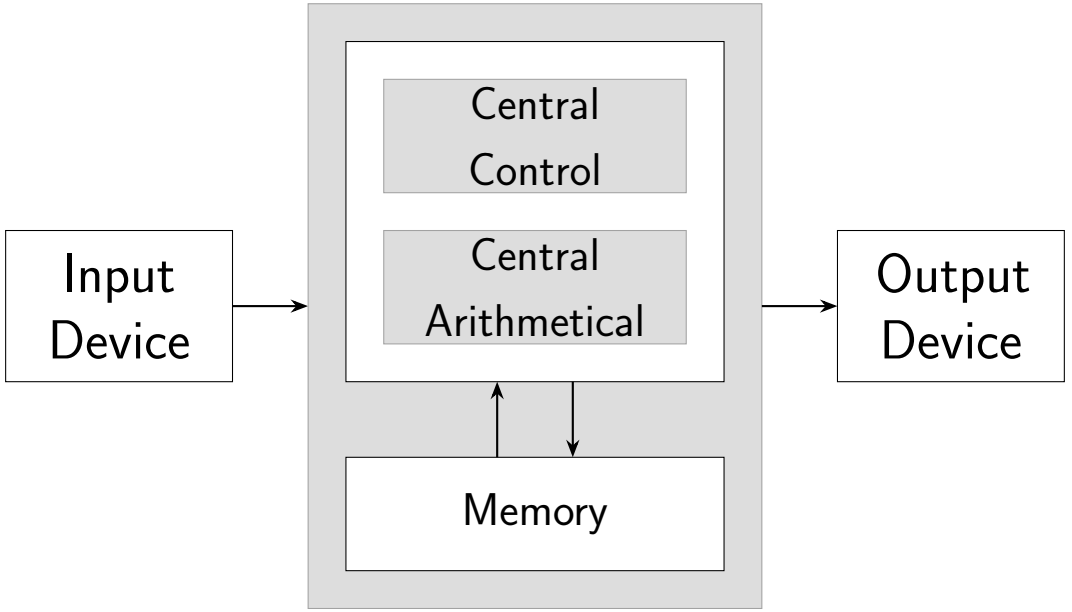
- Load current instruction from memory



Von Neumann Architecture

Control Flow

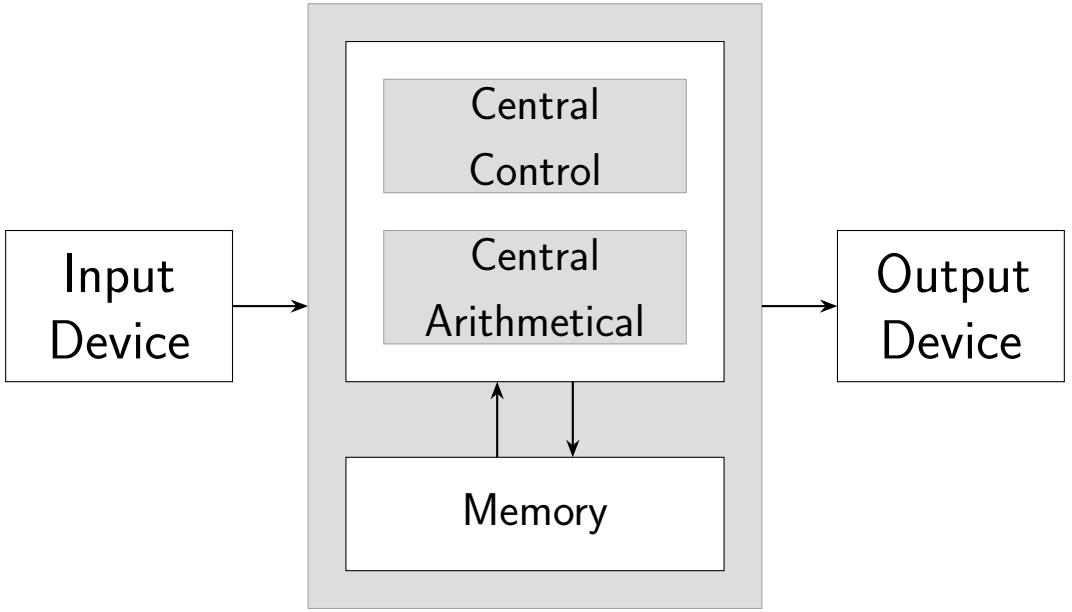
- Load current instruction from memory
- Store instruction in control register



Von Neumann Architecture

Control Flow

- Load current instruction from memory
- Store instruction in control register
- Decode instruction



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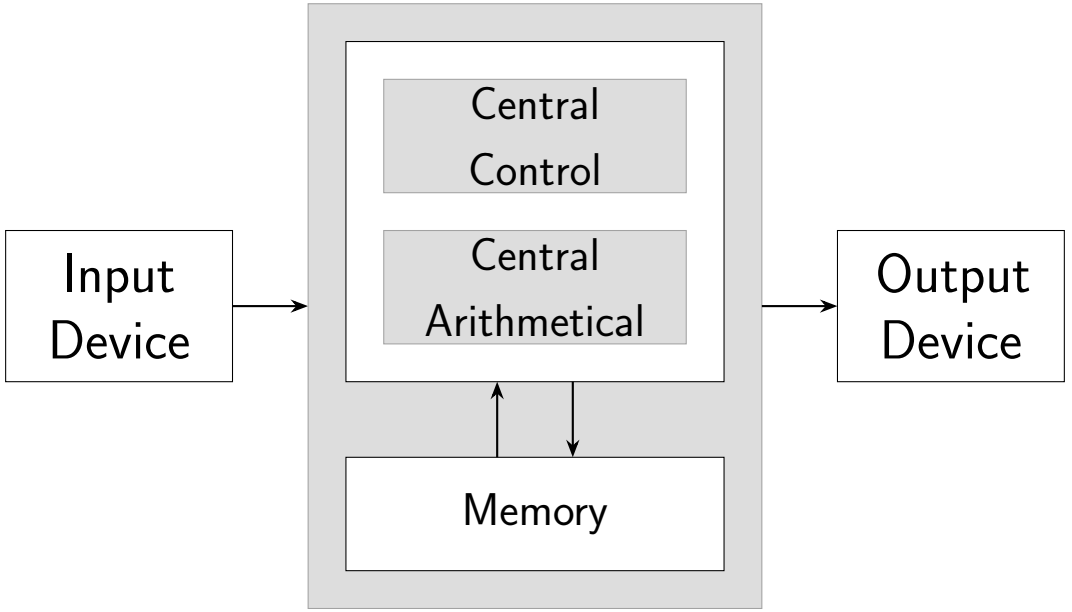

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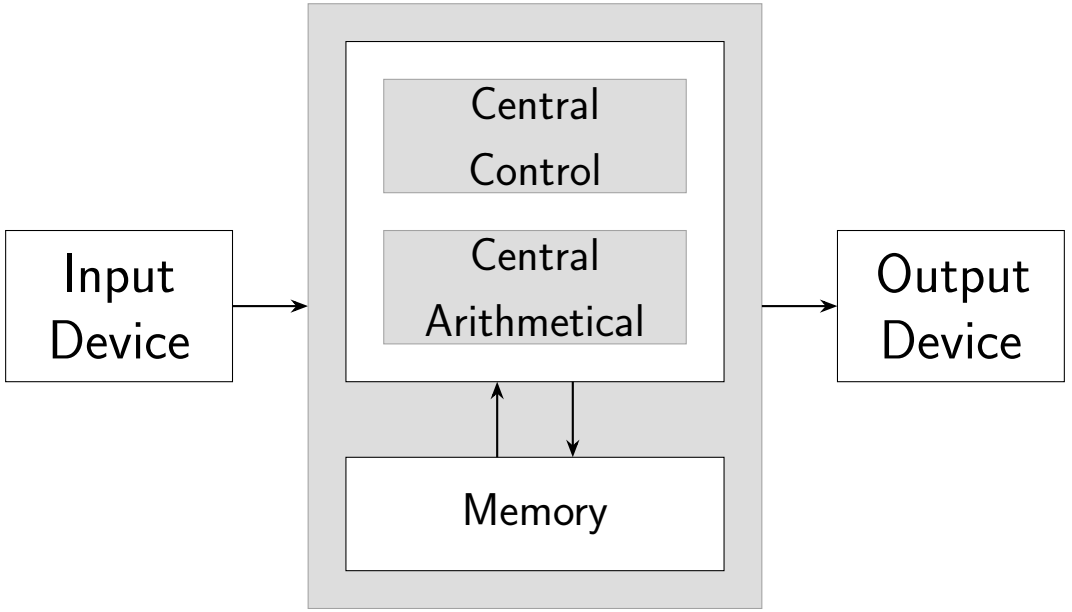

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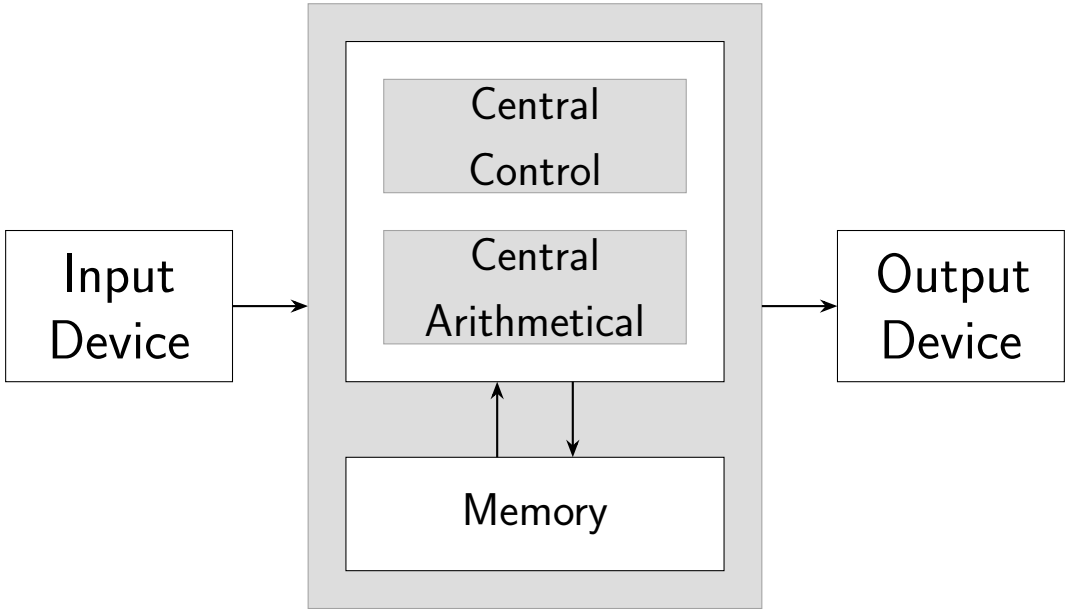

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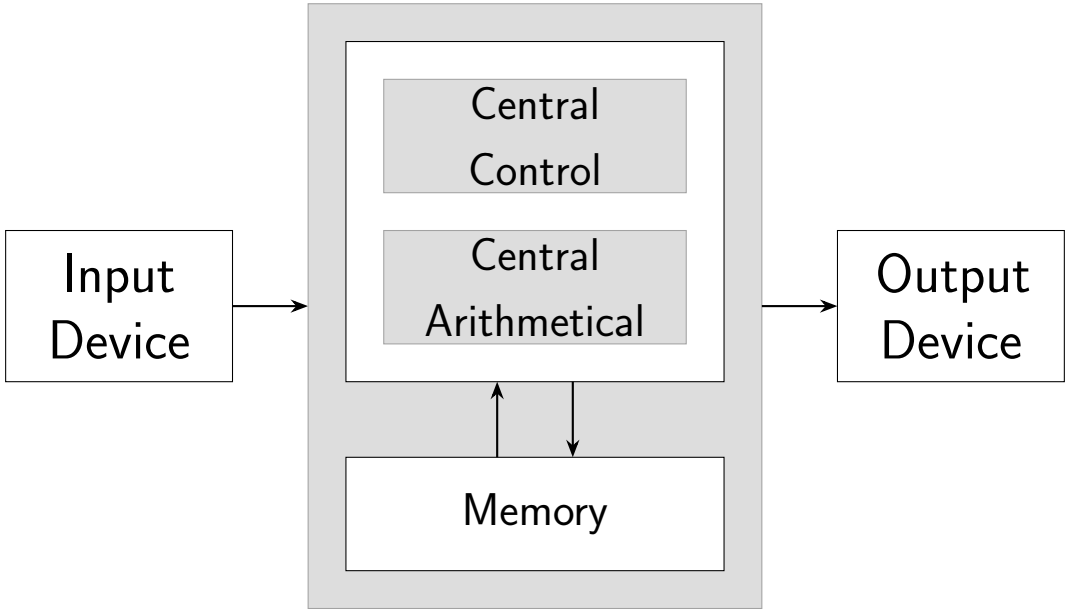

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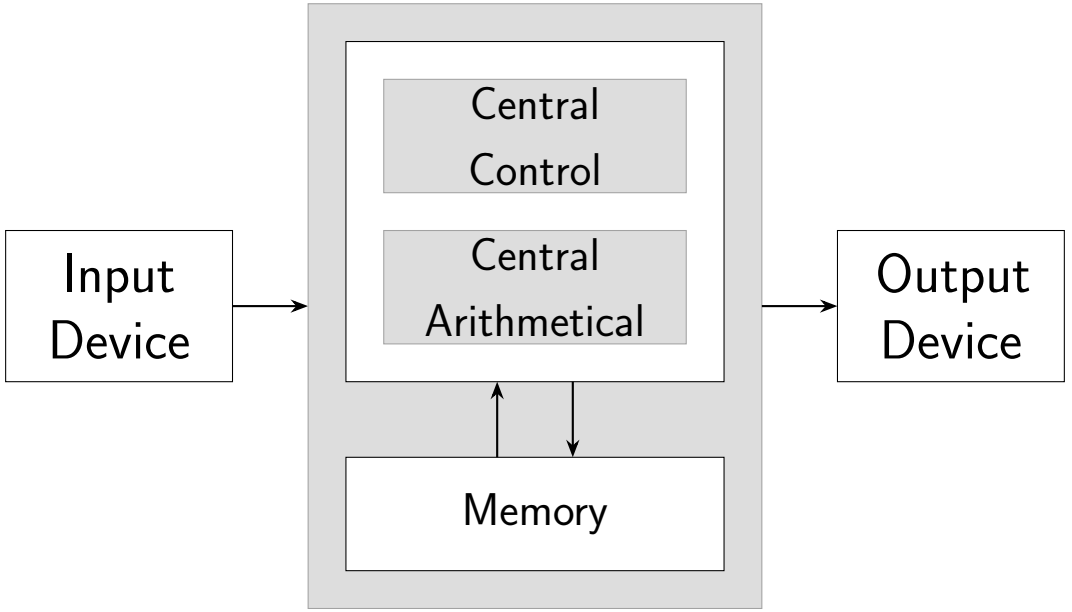

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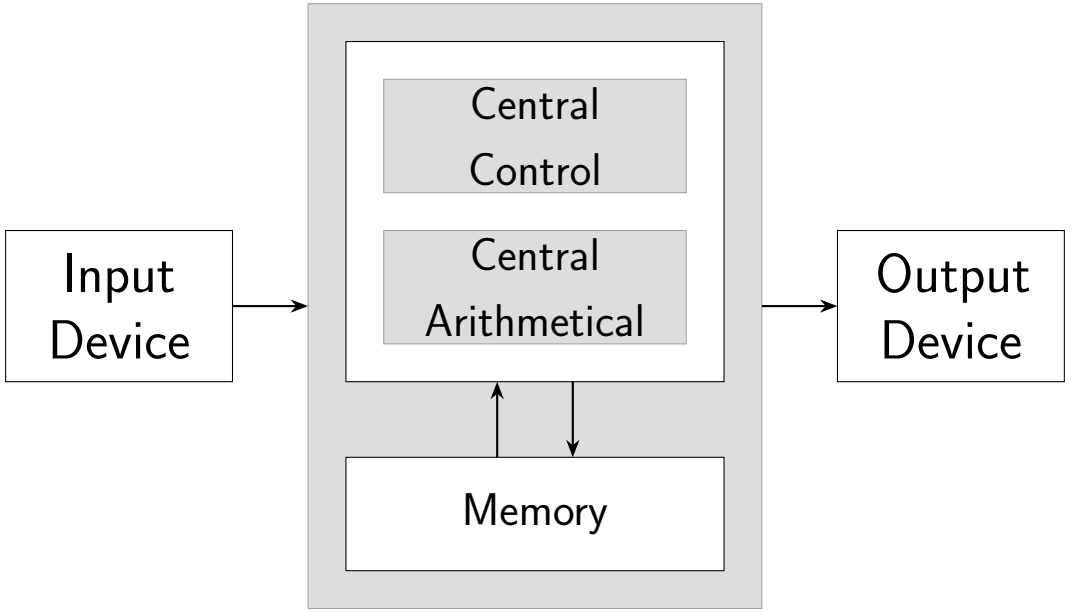

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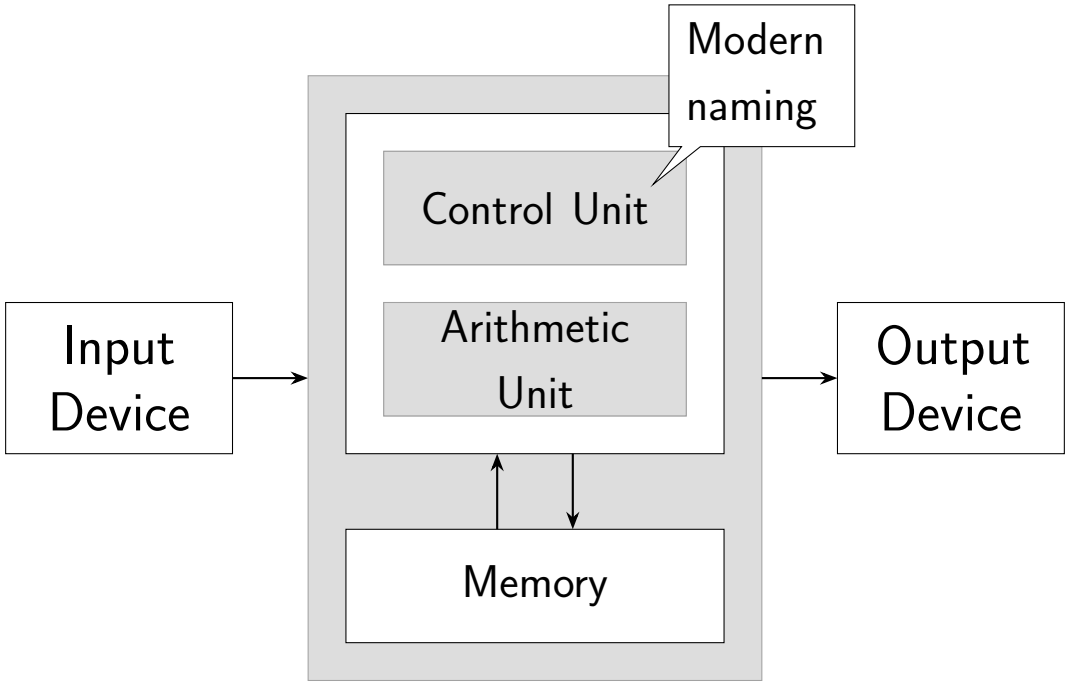
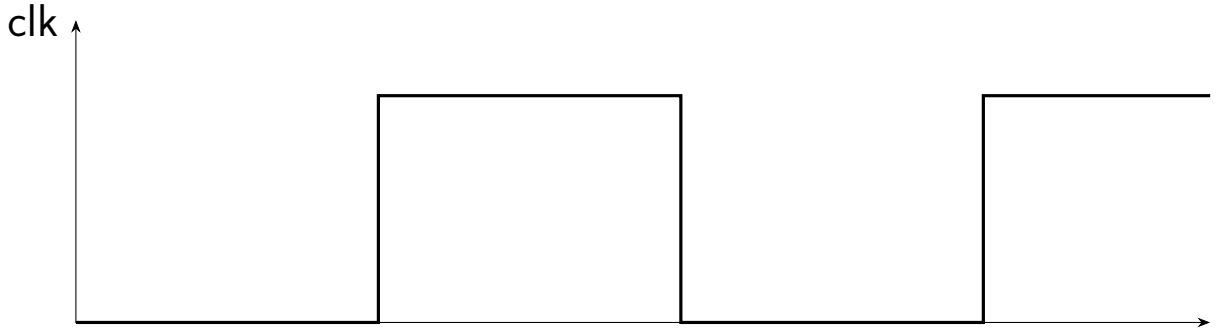


Instruction Processing

Remember: Microprocessor in Computer Engineering (Technische Informatik)



Instruction Processing

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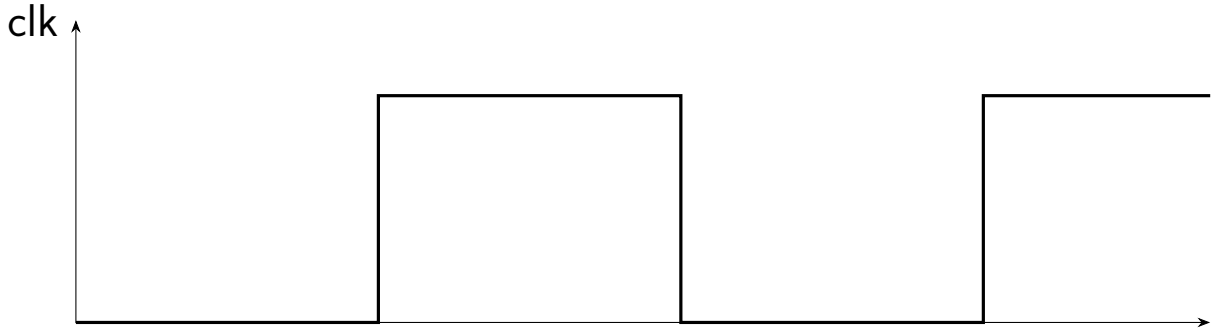
5 phases of execution

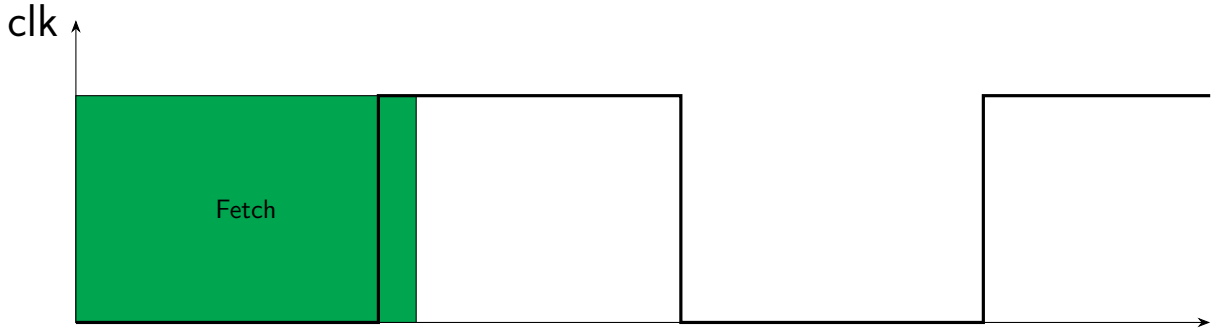


Instruction Processing

Remember: Microprocessor in Computer Engineering (Technische Informatik)

5 phases of execution

- Fetch instruction



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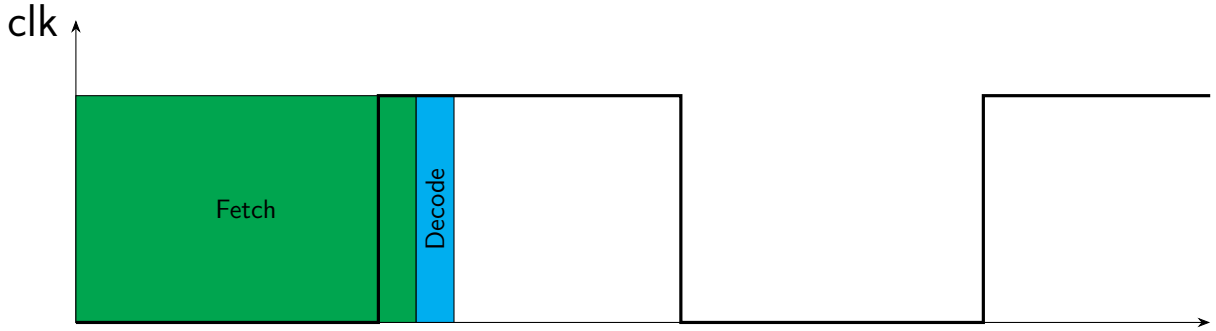

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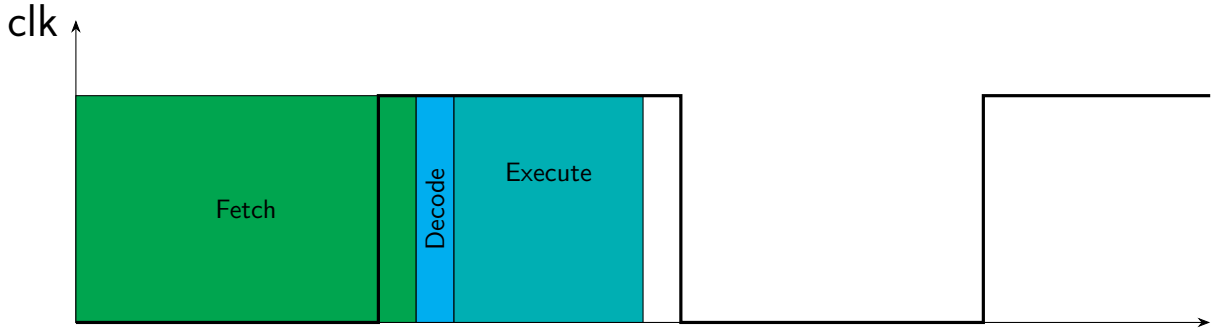

Instruction Processing

Remember: Microprocessor in Computer Engineering (Technische Informatik)

5 phases of execution

- Fetch instruction
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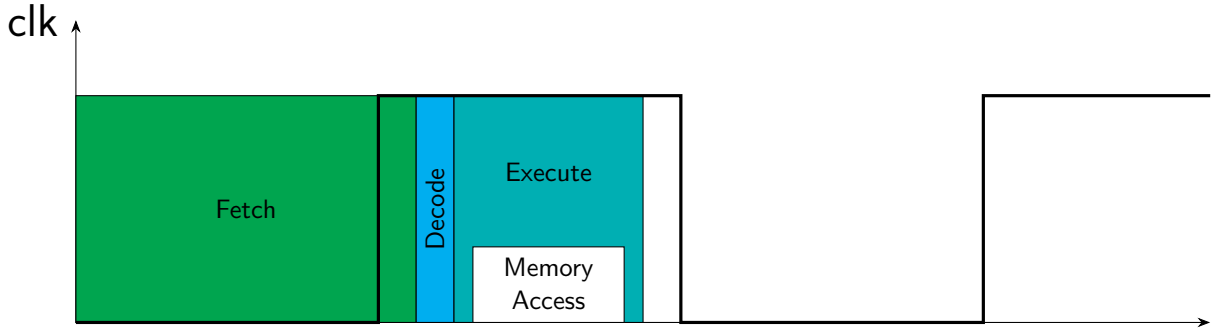
- Execute
- Memory Access



Instruction Processing

Remember: Microprocessor in Computer Engineering (Technische Informatik)

5 phases of execution

- Fetch instruction
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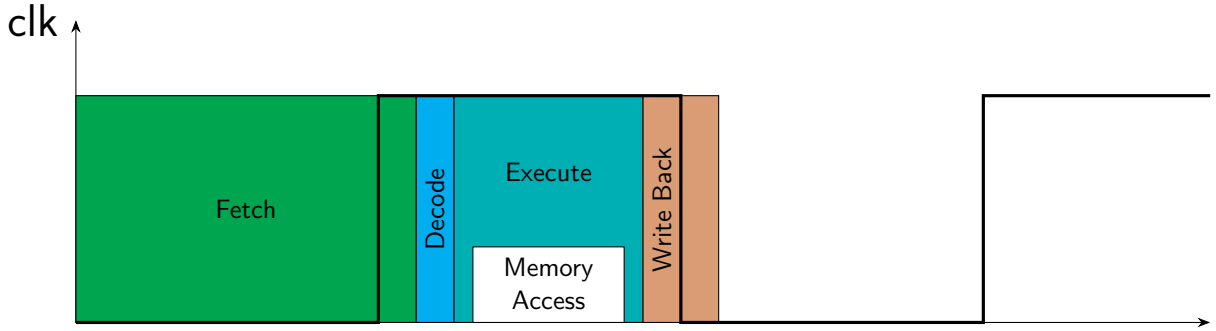
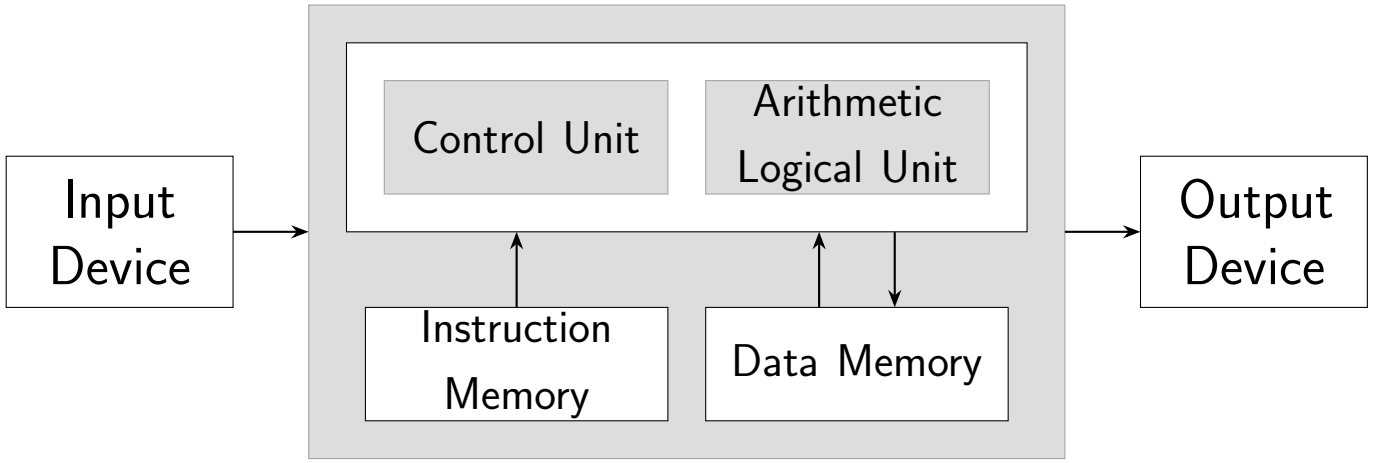
- Execute
- Memory Access
- Write Back



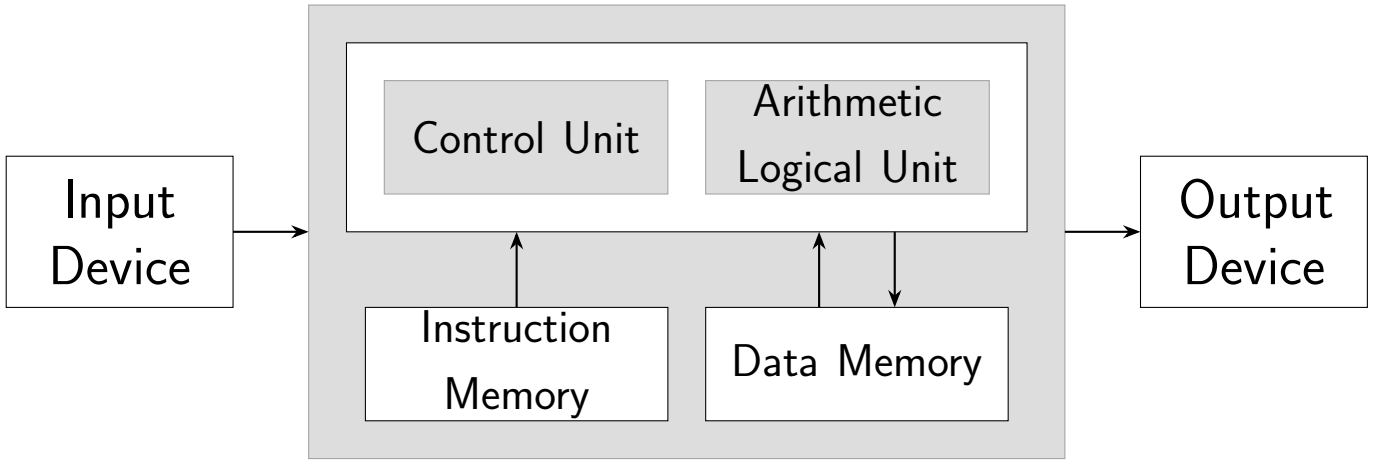
Harvard Architecture

- Separated data and instruction memory



Harvard Architecture

- Separated data and instruction memory
- Today mostly "modified harvard architecture": Separated level 1 caches (see later)



Generic CPU Architecture

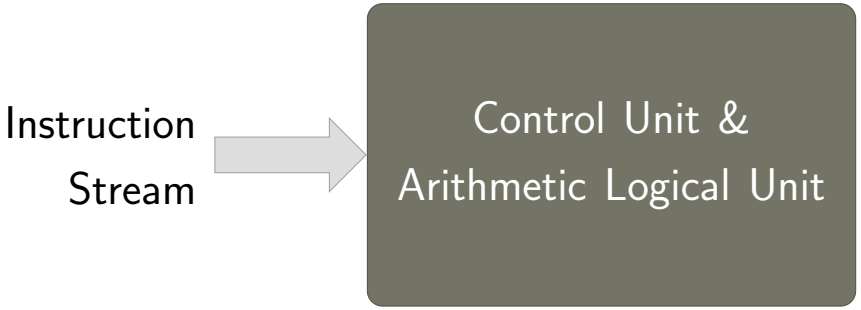
Generic CPU Architecture

- Control unit and ALU as brain and heart of CPU

Control Unit &
Arithmetic Logical Unit

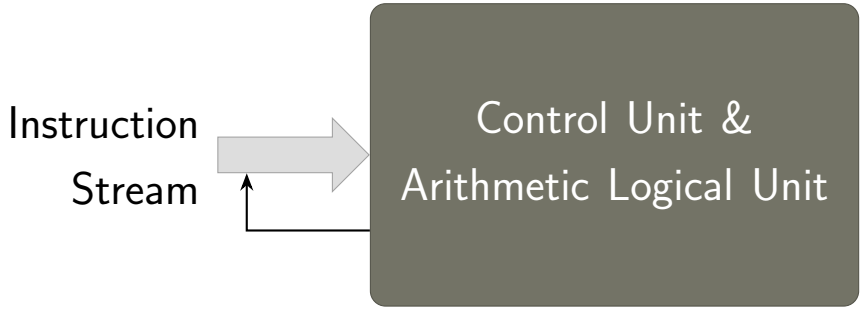
Generic CPU Architecture

- Control unit and ALU as brain and heart of CPU
- Fetch instruction stream



Generic CPU Architecture

- Control unit and ALU as brain and heart of CPU
- Fetch instruction stream
- Diversion of (sequential) instruction stream



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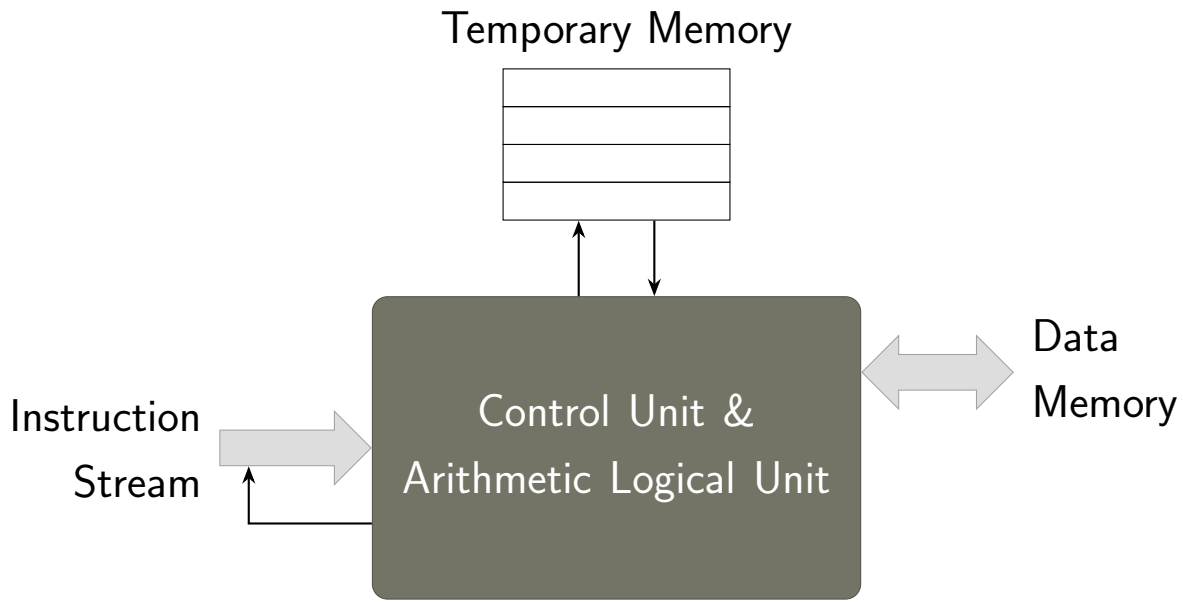
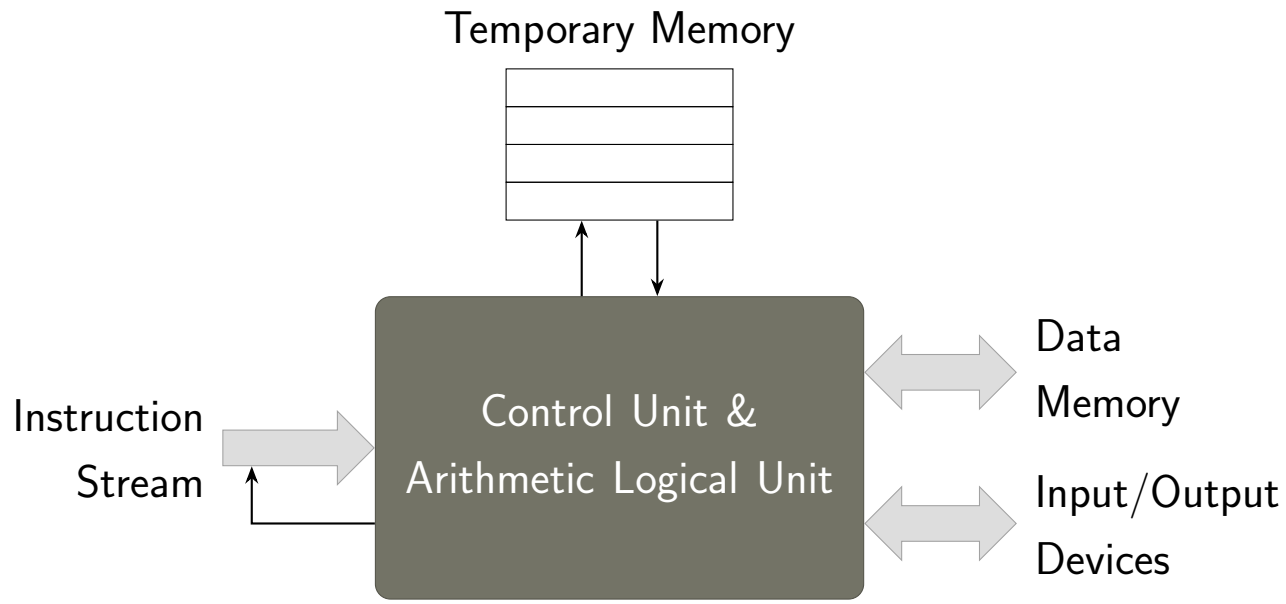
- Temporary memory much faster



Generic CPU Architecture

- Control unit and ALU as brain and heart of CPU
- Fetch instruction stream
- Diversion of (sequential) instruction stream
- Access to data memory
- Temporary memory much faster
- Often I/O interface



Instruction Set Architecture vs. Microarchitecture

Instruction Set Architecture (ISA)

- General operation of a CPU

Microarchitecture

Instruction Set Architecture vs. Microarchitecture

Instruction Set Architecture (ISA)

- General operation of a CPU
- "Contract" with programmer/compiler

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Instruction Set Architecture vs. Microarchitecture

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Instruction Set Architecture vs. Microarchitecture

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Instruction Set Architecture vs. Microarchitecture

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- General operation of a CPU
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Microarchitecture

- Actual implementation of the ISA

Instruction Set Architecture vs. Microarchitecture

Instruction Set Architecture (ISA)

- General operation of a CPU
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Microarchitecture

- Actual implementation of the ISA
- Many design alternatives and optimizations

Instruction Set Architecture vs. Microarchitecture

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- General operation of a CPU
- "Contract" with programmer/compiler
- Defines instructions, states, memory access and interface to outside world
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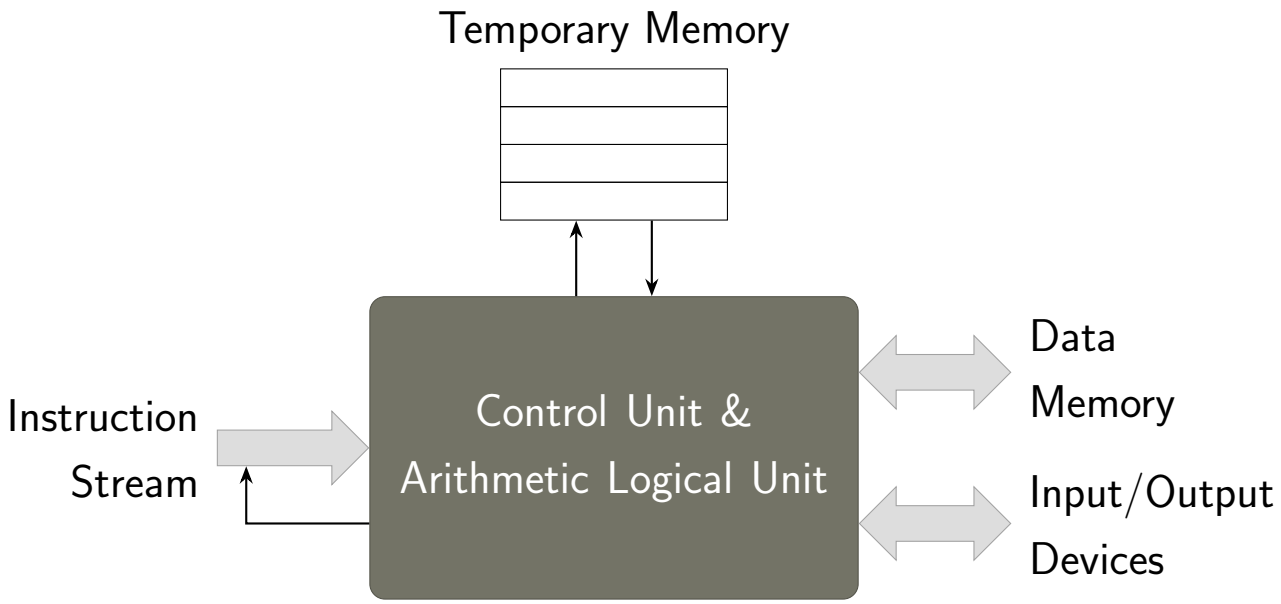
Microarchitecture

- Actual implementation of the ISA
- Many design alternatives and optimizations
- Must obey rules set out by ISA

Instruction Set Architecture vs. Microarchitecture



Examples: ISA and Microarchitecture 1/3

ISA	Manufacturer	Microarchitecture/Product
x86	Intel	8086, 80186, 80286, 80386, 80486, P5 (Pentium), P6 (Pentium II/III)
	AMD	8086, Am386, K5, K6, Athlon
	VIA/Cyrix	C3, C7

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ia64	Intel/HP	Itanium, Itanium 2, Itanium 9300

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	VIA/Cyrix	C3, C7
ia64	Intel/HP	Itanium, Itanium 2, Itanium 9300
x86-64	AMD	Opteron, Athlon 64, Turion, ..., Ryzen/Epyc
	Intel	Pentium 4, Xeon, Atom, Core 2, ..., Cannon Lake (e.g. Core i3 8121U)

Examples: ISA and Microarchitecture 2/3

ISA	Manufacturer	Microarchitecture/Product
ARMv2, .., ARMv6	ARM	ARM1, ARM2, ARM6, ARM7, .. ARM11
	DEC	StrongARM
	Intel	Xscale

Examples: ISA and Microarchitecture 2/3

ISA	Manufacturer	Microarchitecture/Product
ARMv2, .., ARMv6	ARM	ARM1, ARM2, ARM6, ARM7, .. ARM11
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	Intel	Xscale
ARMv7-A	ARM	Cortex-A5, Cortex-A7, ..., Cortex-A17
	Qualcomm	Krait, Scorpion
	Apple	A6

Examples: ISA and Microarchitecture 2/3

ISA	Manufacturer	Microarchitecture/Product
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	Qualcomm	Krait, Scorpion
	Apple	A6
ARMv8-A	ARM	Cortex-A35, Cortex-A53, ..., Cortex-A76
	Qualcomm	Kryo
	Apple	A7, A8, A9, A10, A11, A12
	Samsung	M1, M2

Examples: ISA and Microarchitecture 3/3

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VAX, Alpha, PA-RISC, AVR, ...		

RISC-V Instruction Set Architecture

- Started as academic project at UC Berkeley (Asanovic/Patterson)
- Open instruction set architecture
- Widely adopted in industry
- Clean and clear ISA
- Open and proprietary implementations

➔ Used in course labs

INSTRUCTION SET ARCHITECTURE

Example: 

Register and Register Files

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Example: `a = b + c - d`

Instruction Coding RISC-V®

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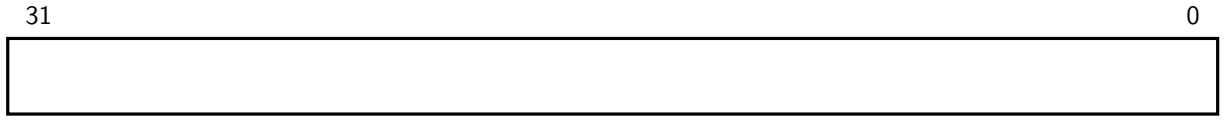

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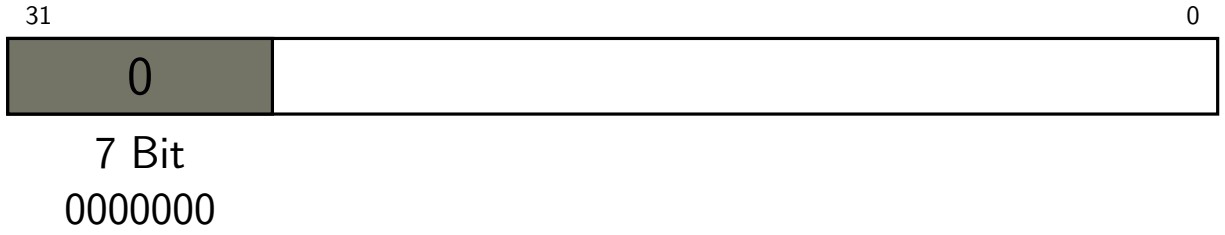

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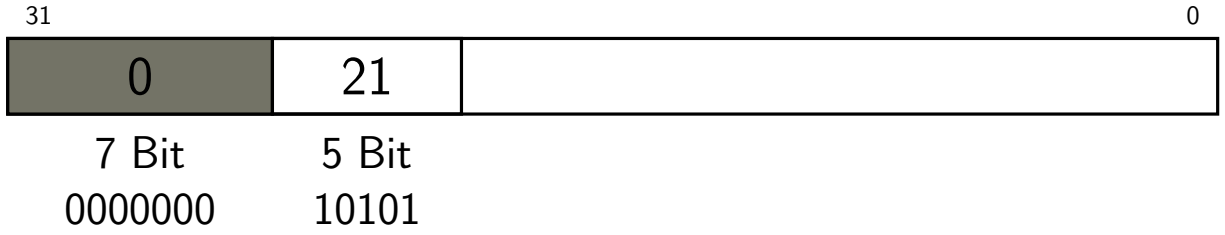

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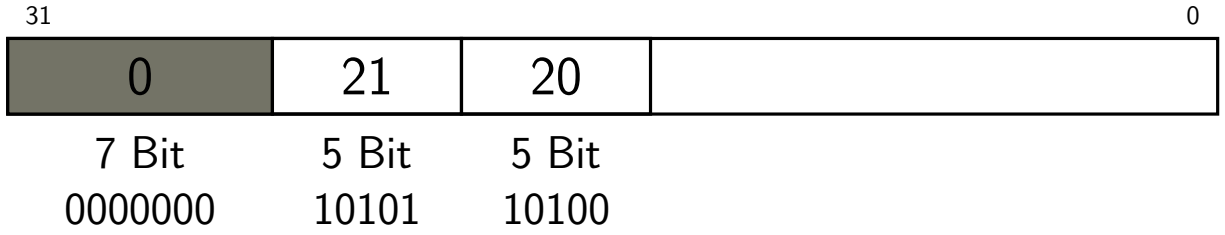

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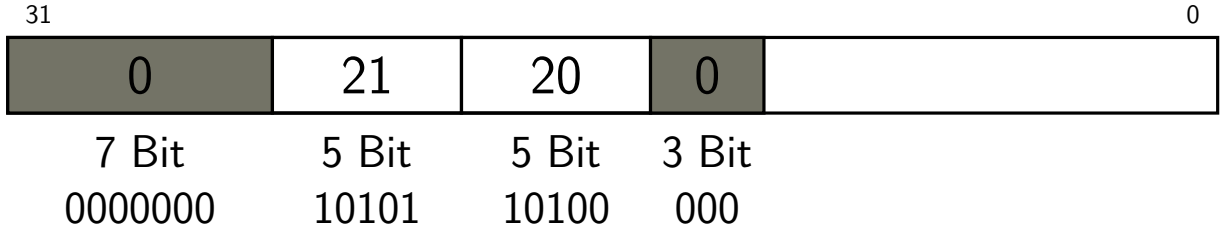

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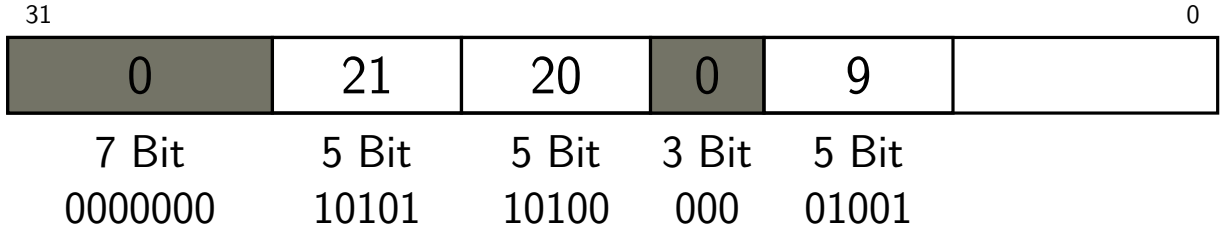

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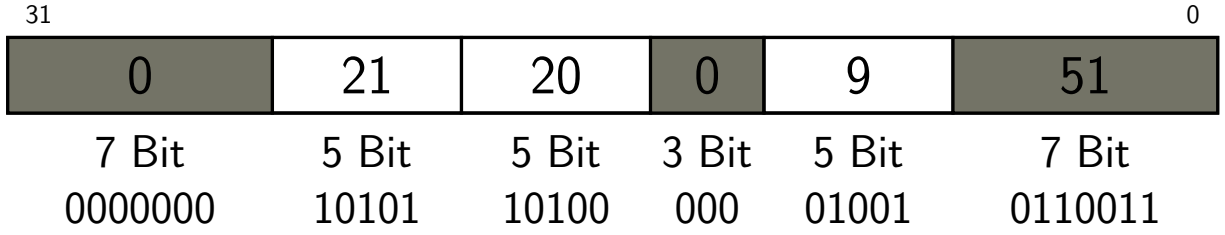

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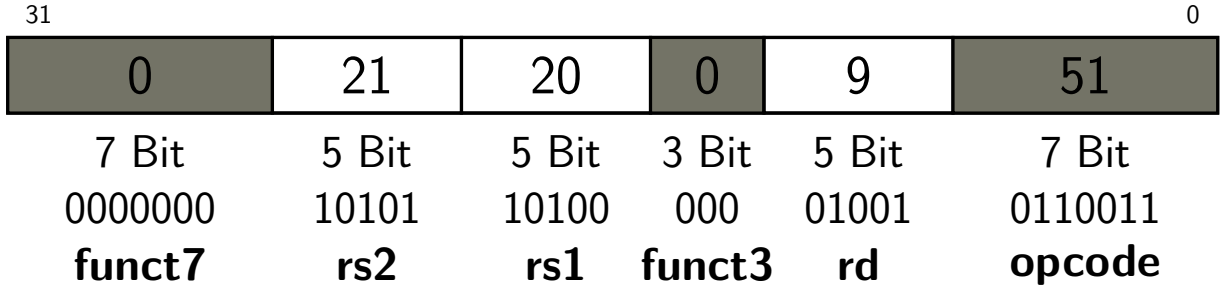

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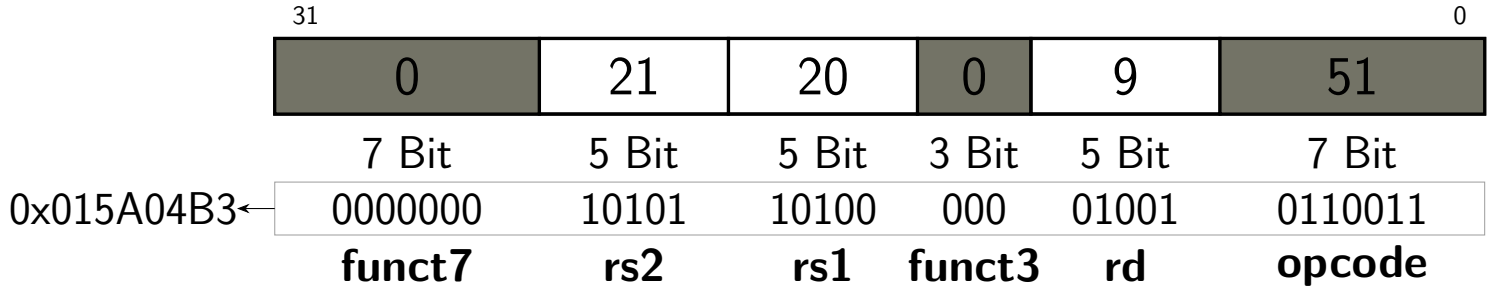

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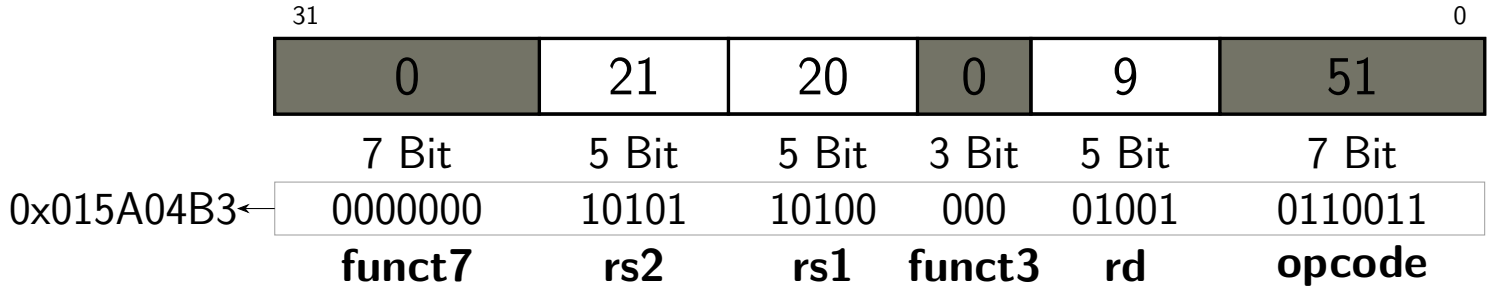

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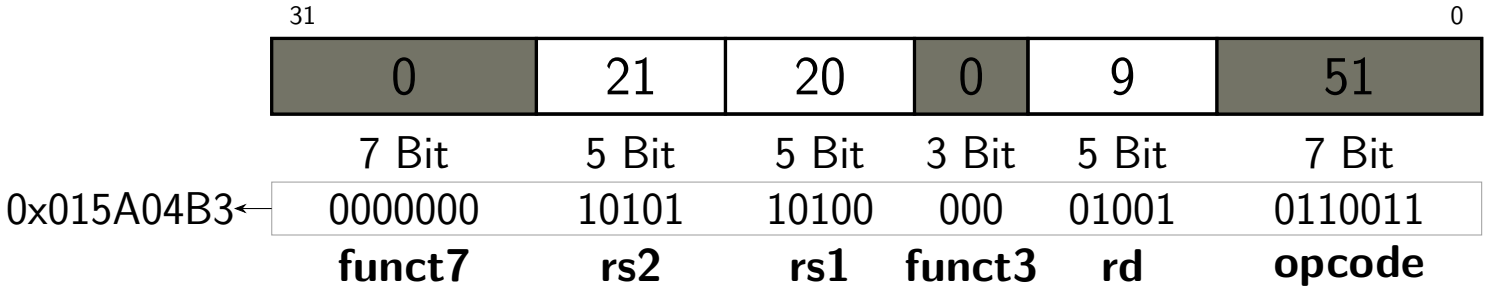

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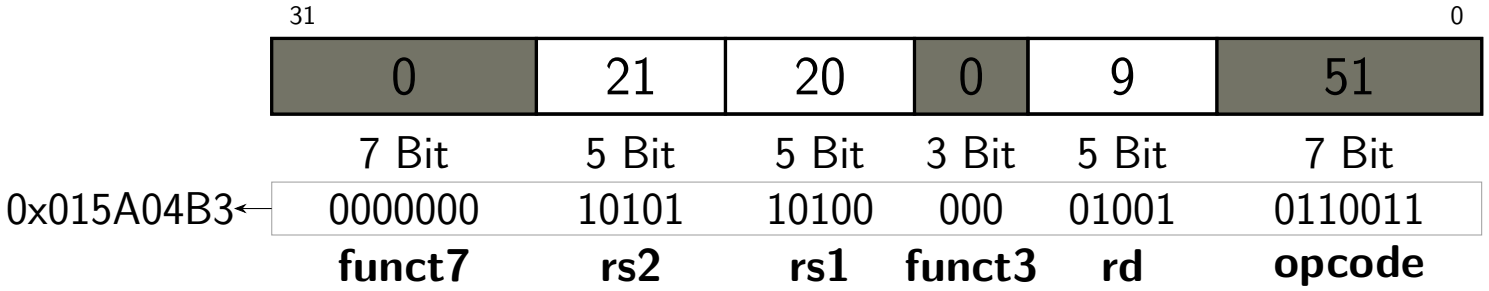

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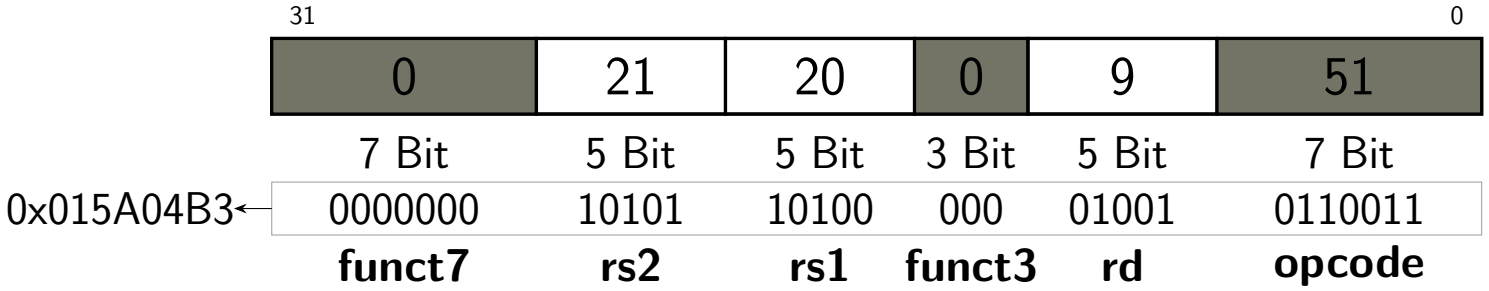

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Immediate Instruction Coding RISC-V®

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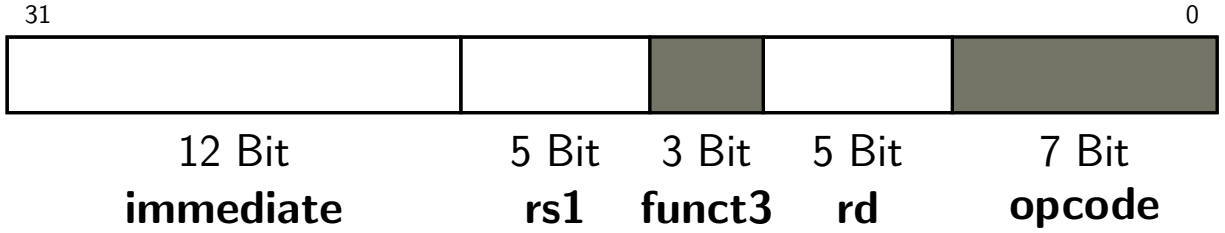

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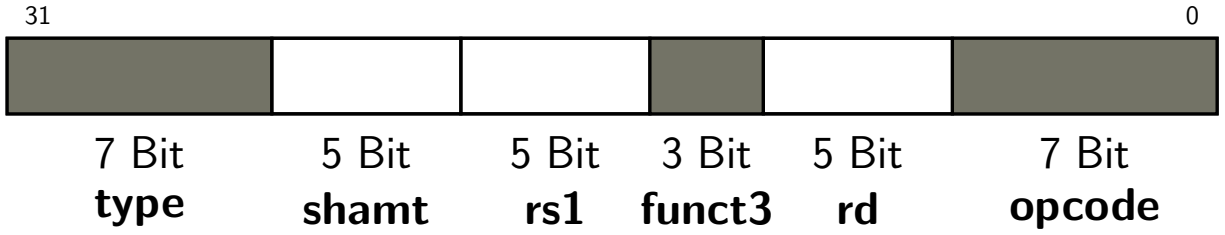

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- RISC-V: Compact (C) ISA extension, ARM: Thumb ISA extension

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- Examples: x86, most computers until 1990s

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- Under the hood modern CISC processors are actually RISC processors:
  newline Translation of CISC commands into RISC microcode

Instruction Set Complexity: Video

Krste Asanovic - RISC-V: Instruction Sets Want To Be Free, MeetBSD 2016

`https://youtu.be/QTYiH1Y5UV0?t=371`

(6:11 to 9:16 are of interest in this context, but the entire video is a great watch!)

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Properties of memory access (endianess, alignment) and operation (adressing modes, instructions)

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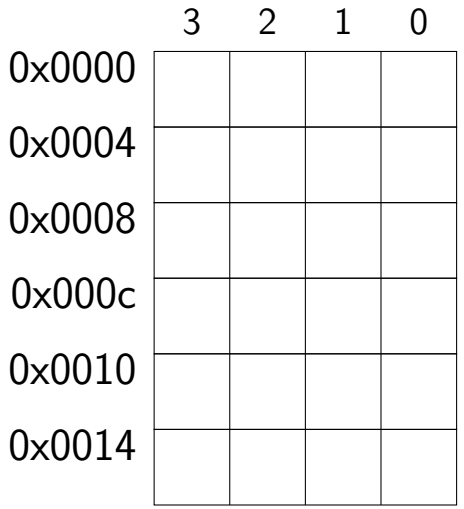
Alignment: Example

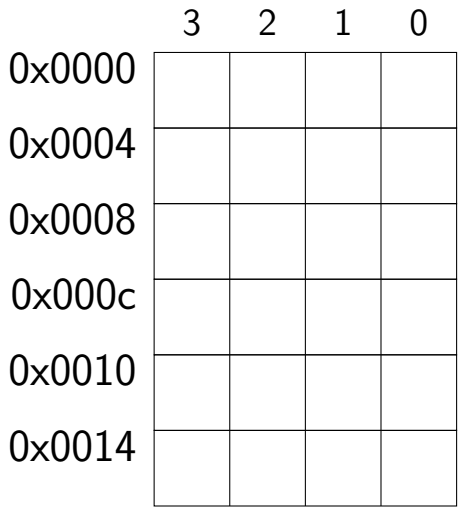


Memory

Alignment: Example

```
struct {
  uint32_t A;
  uint8_t B;
  uint32_t C;
};
```

Data Structure



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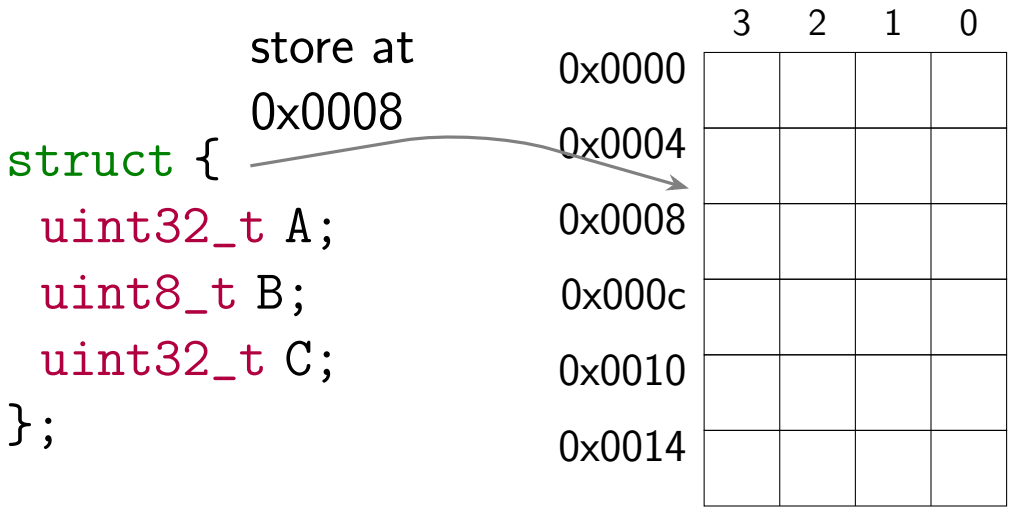

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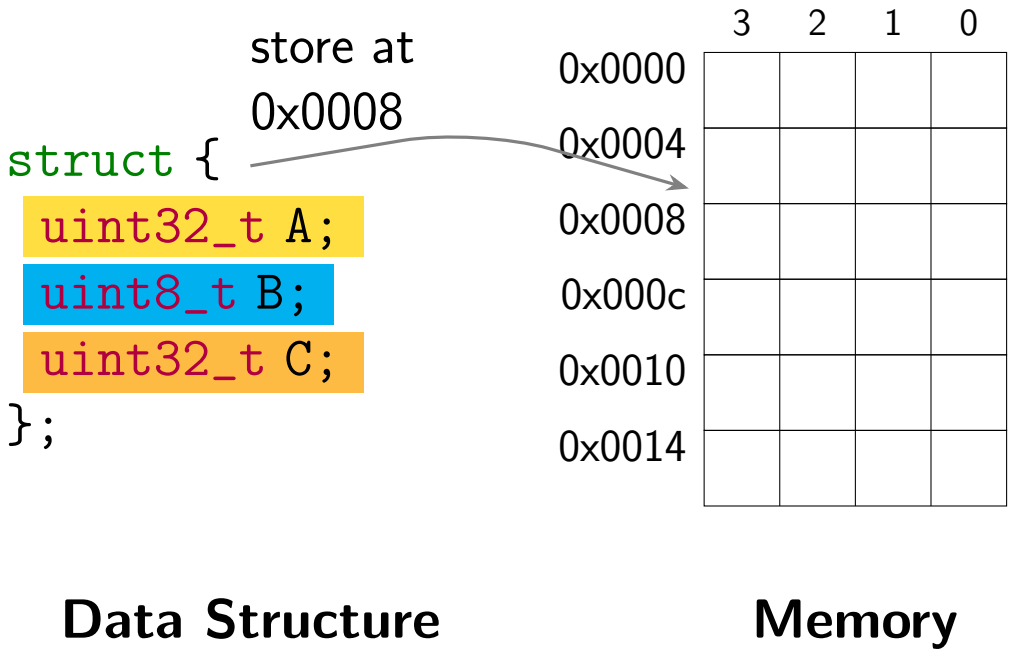

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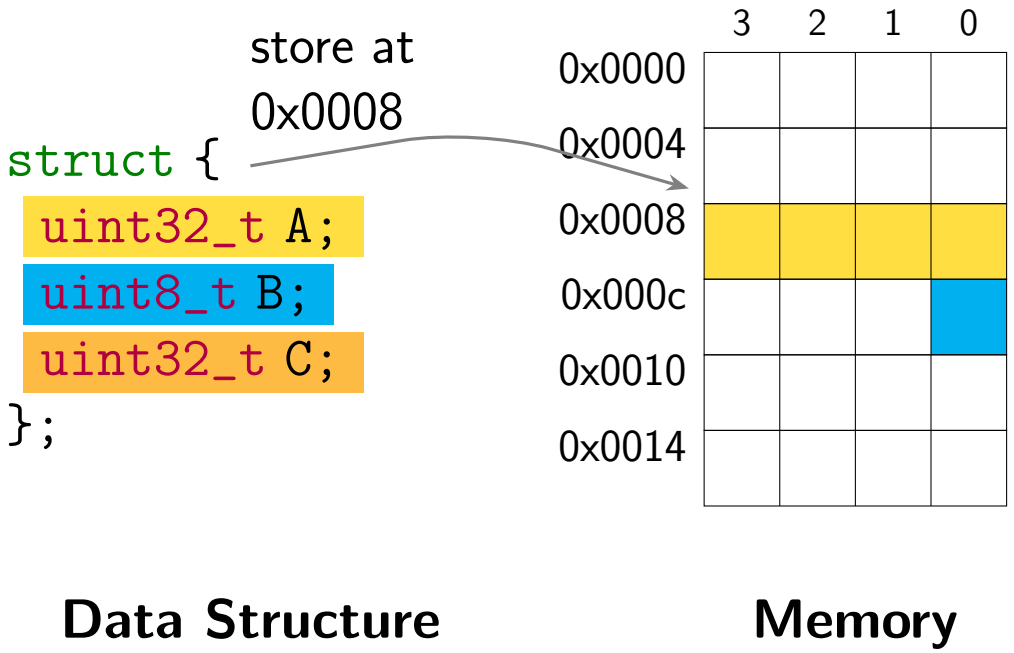

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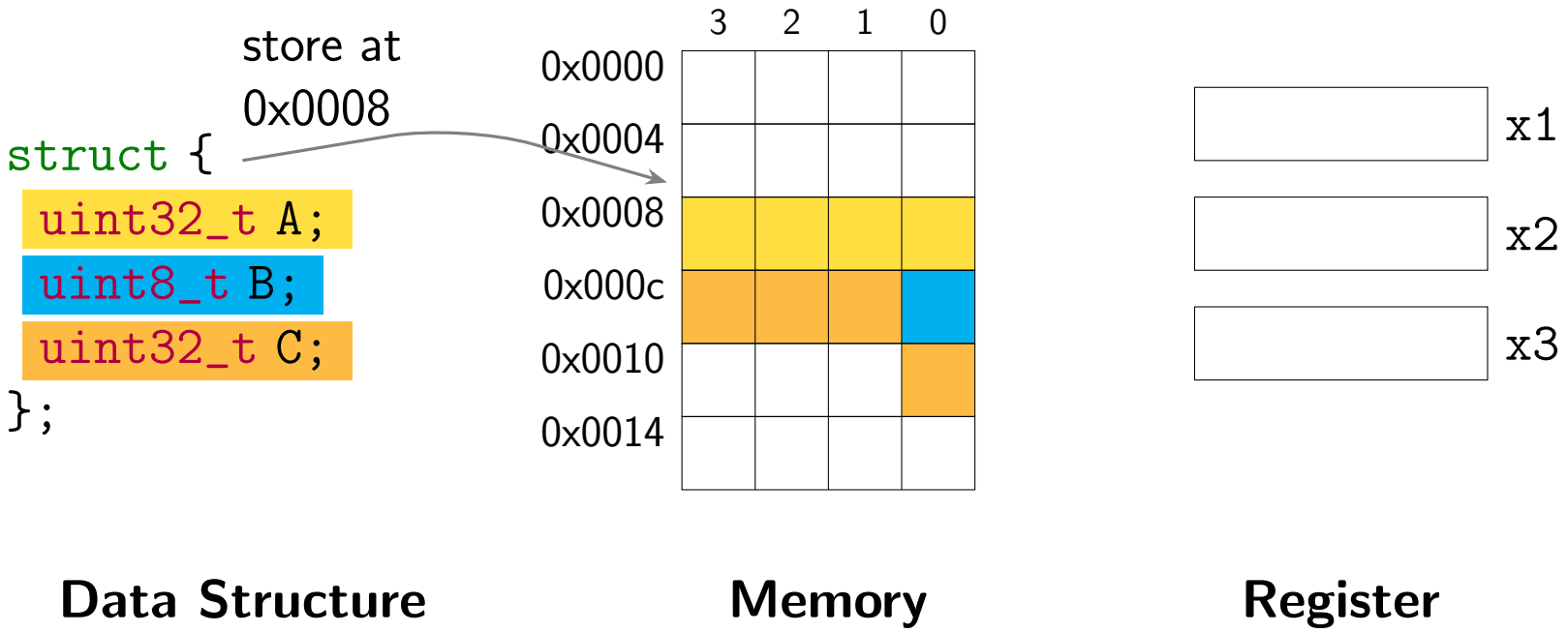

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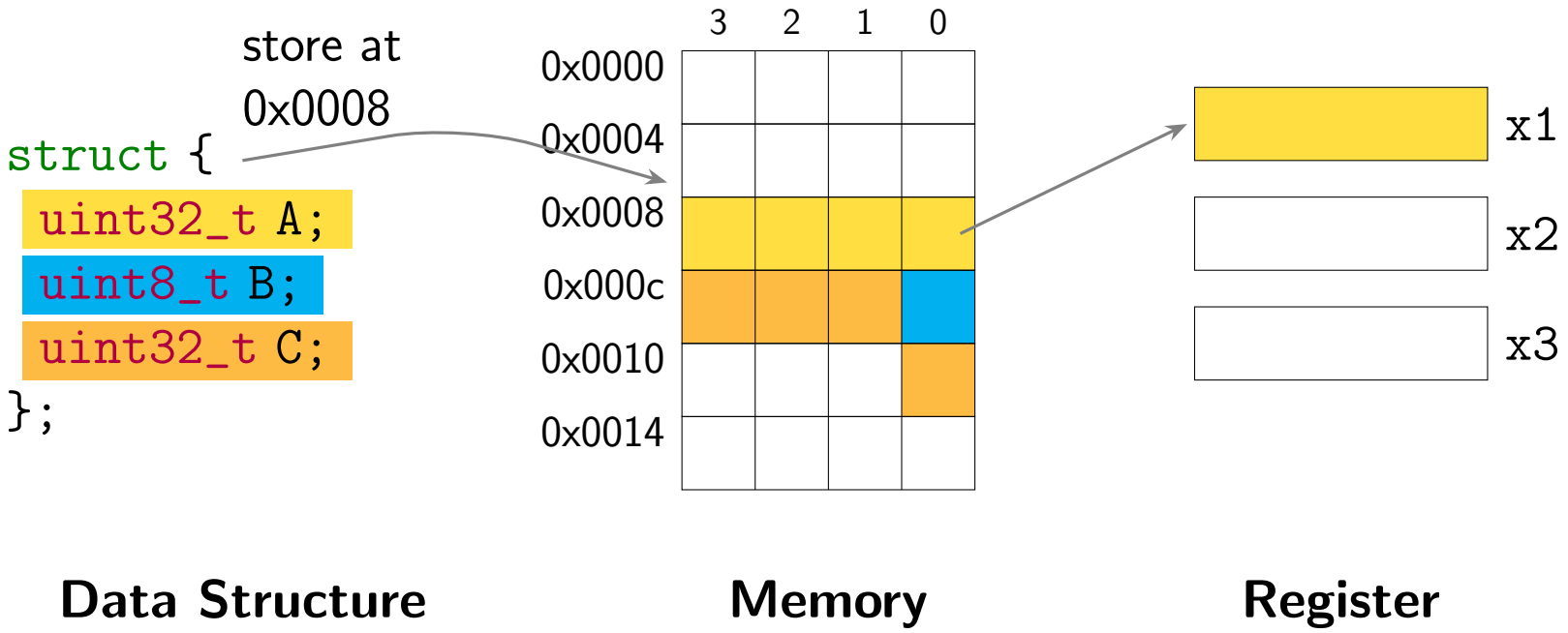

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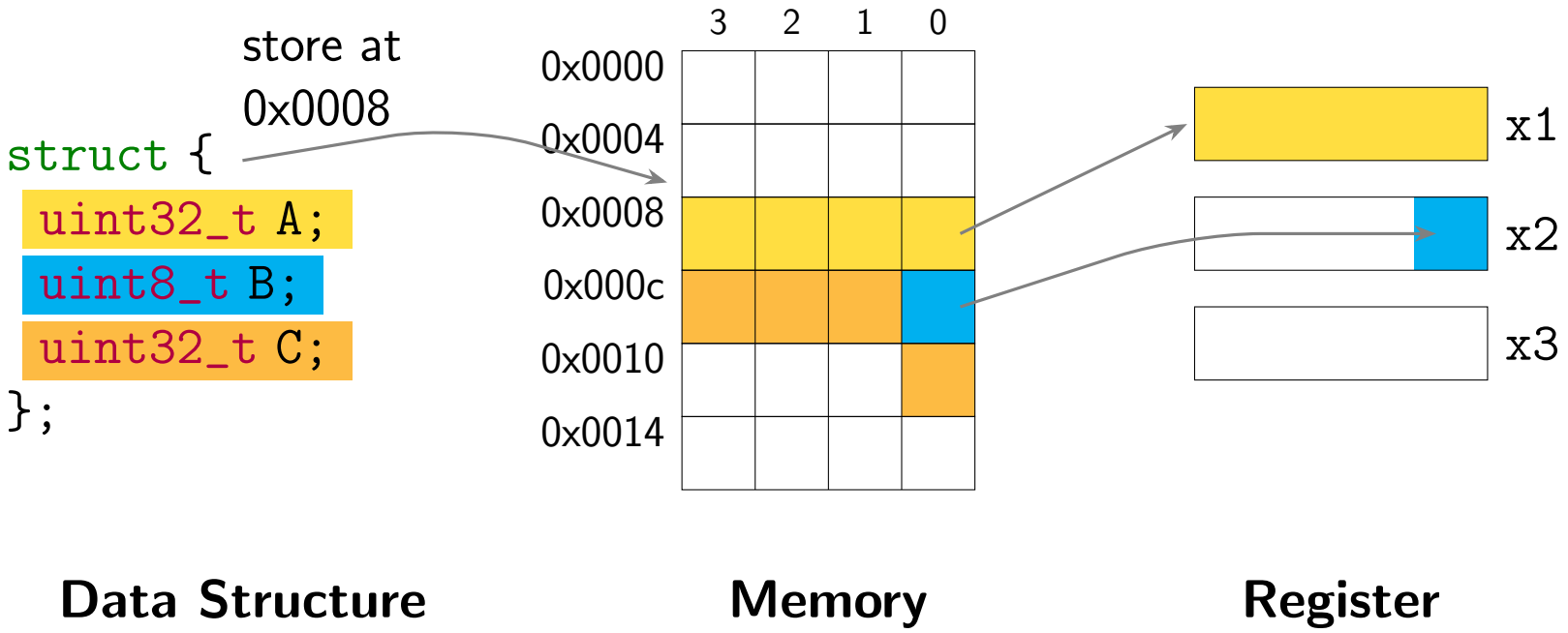

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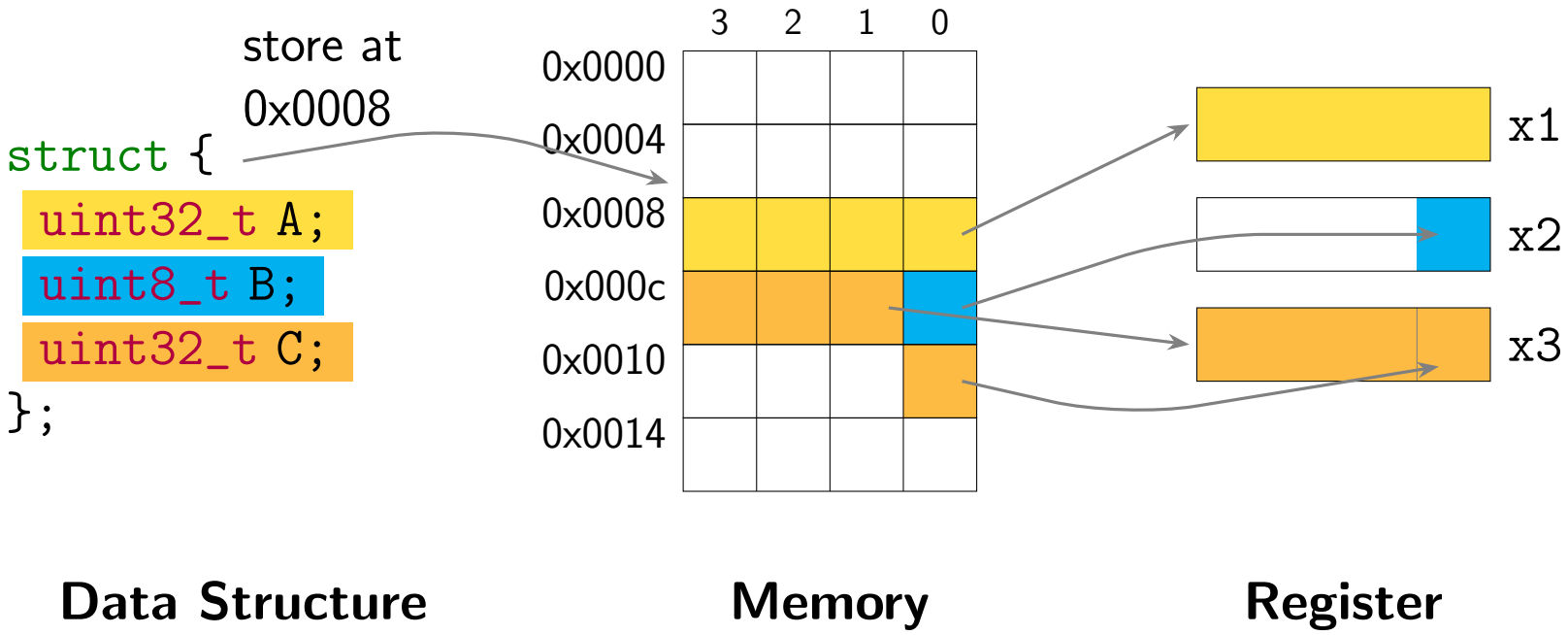

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RISC concept limits memory operands to transport operations (load-store architecture)

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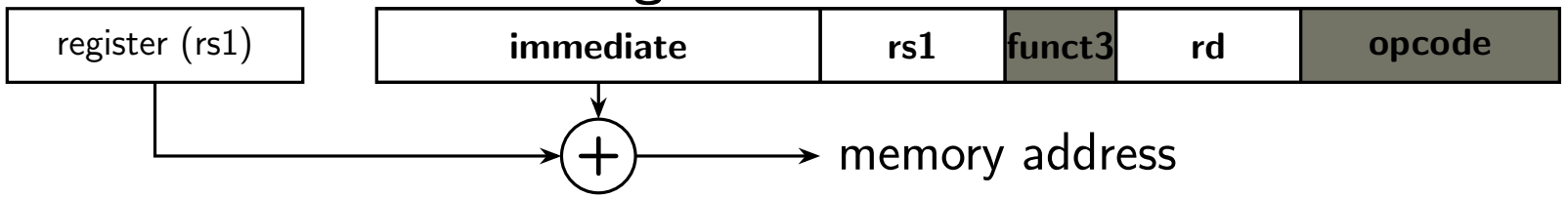

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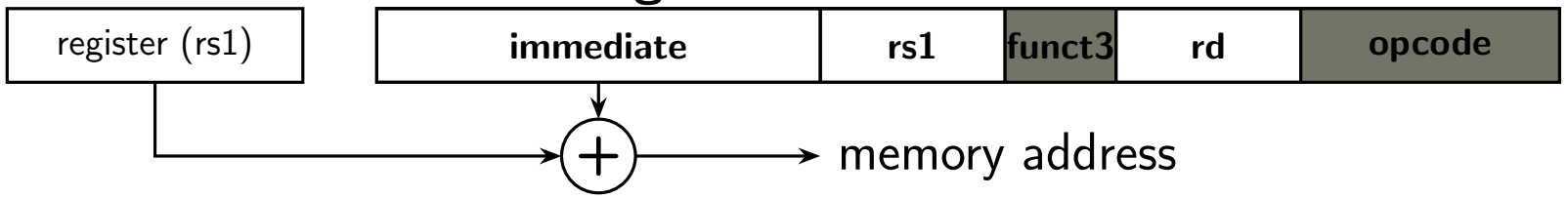

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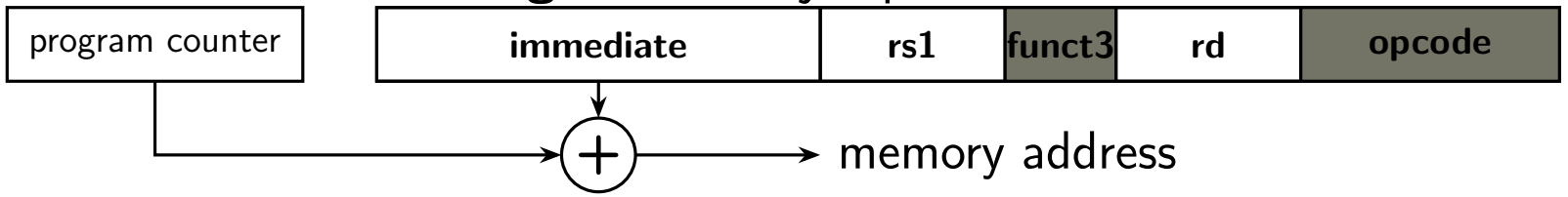

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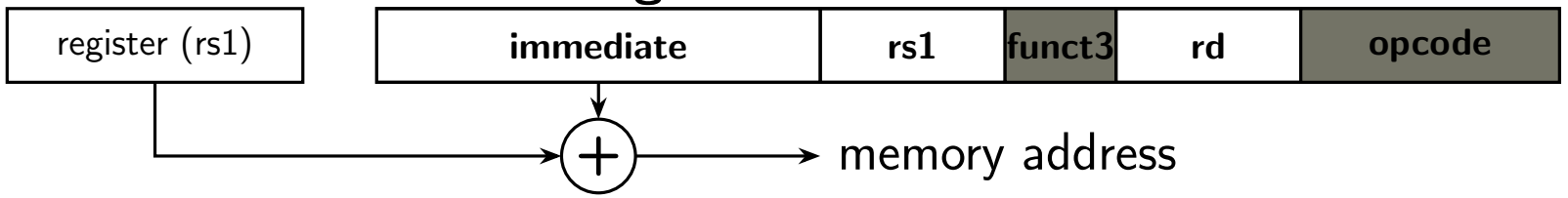

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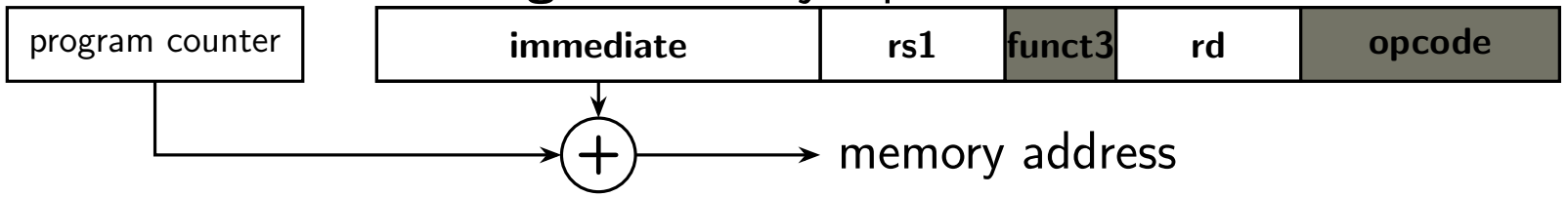

No alignment required, either hardware supports misaligned or software emulation

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- `lhu rd, imm(rs1)` (rd = {0,Mem[rs1+imm](15:0)})
- `lw rd, imm(rs1)` (rd = {sign,Mem[rs1+imm](31:0)})
- `lwu rd, imm(rs1)` (rd = {0,Mem[rs1+imm](31:0)})
- `ld rd, imm(rs1)` (rd = {sign,Mem[rs1+imm](7:0)})

Memory Access: Load Instructions

Different granularities (byte, half-word, word, double-word) and signedness

- `lb rd, imm(rs1)` (rd = {sign,Mem[rs1+imm](7:0)})
- `lbu rd, imm(rs1)` (rd = {0,Mem[rs1+imm](7:0)})
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Immediate ("I") instruction coding

Memory Access: Store Instructions

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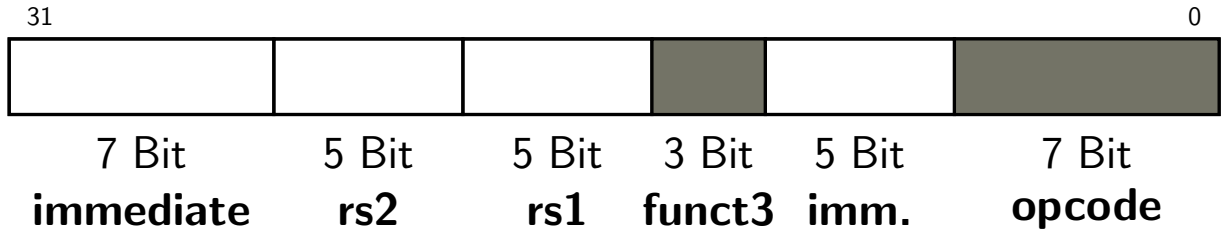

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Comparisons are needed in programming (depend execution on data)

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```
cmp  r1, r2
subgt r1, r1, r2
```

ARM Predication

Comparison in RISC-V®

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RISC-V does not have condition codes or predication

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- Observation: Other comparisons (==, <=, >=) commonly used with branches

Control Transfer Instructions

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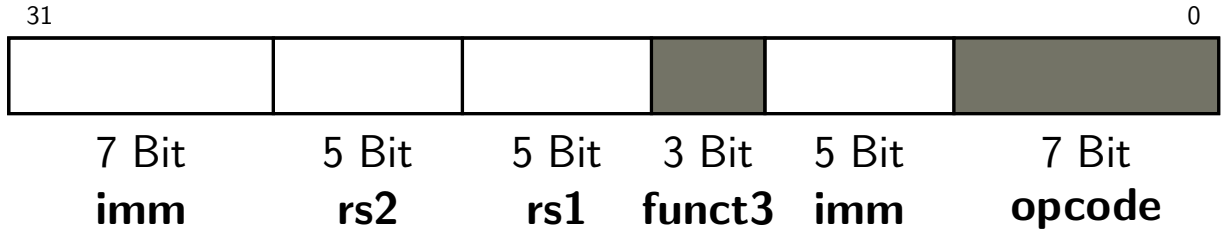
"B" Instruction format



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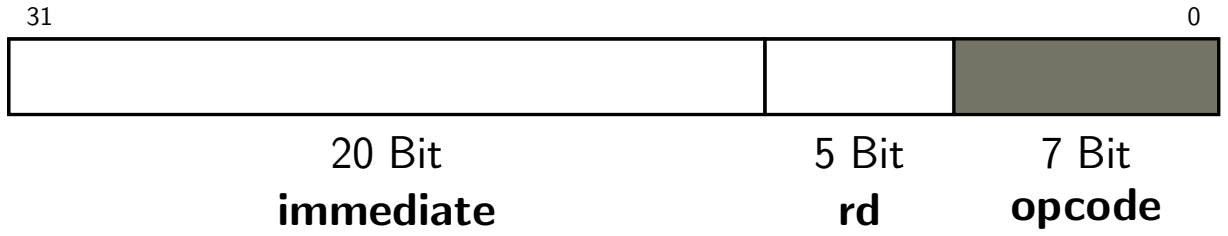
"J" format for `jal`, (known) "I" format for `jalr`



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ISAs provide operations for **constant/address formation** to solve the issue

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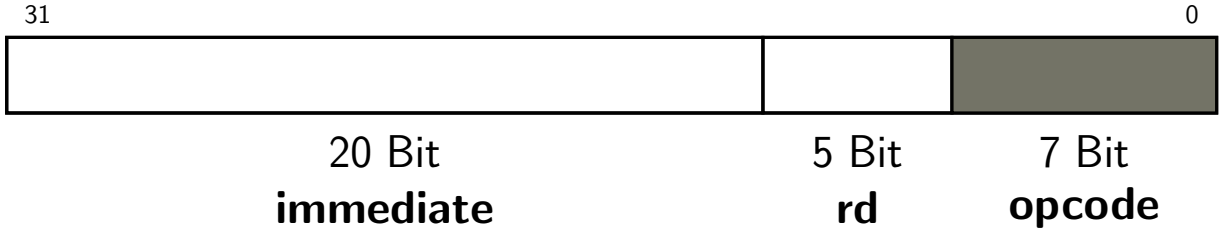
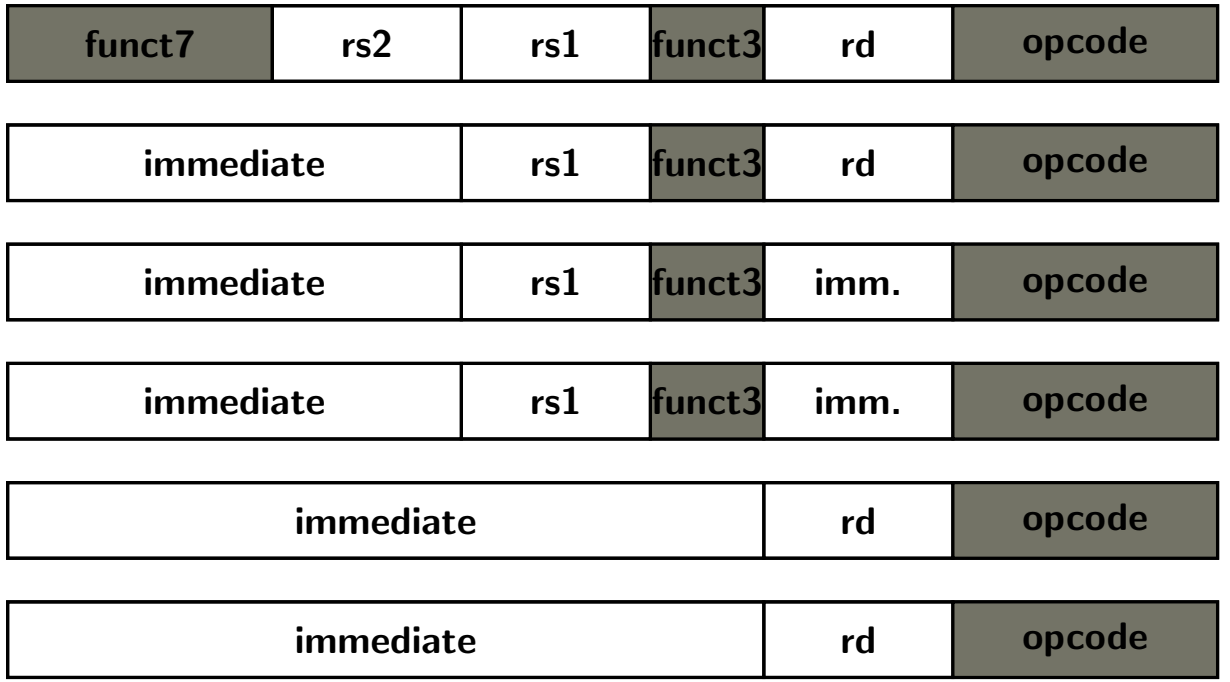


Summary of instruction formats



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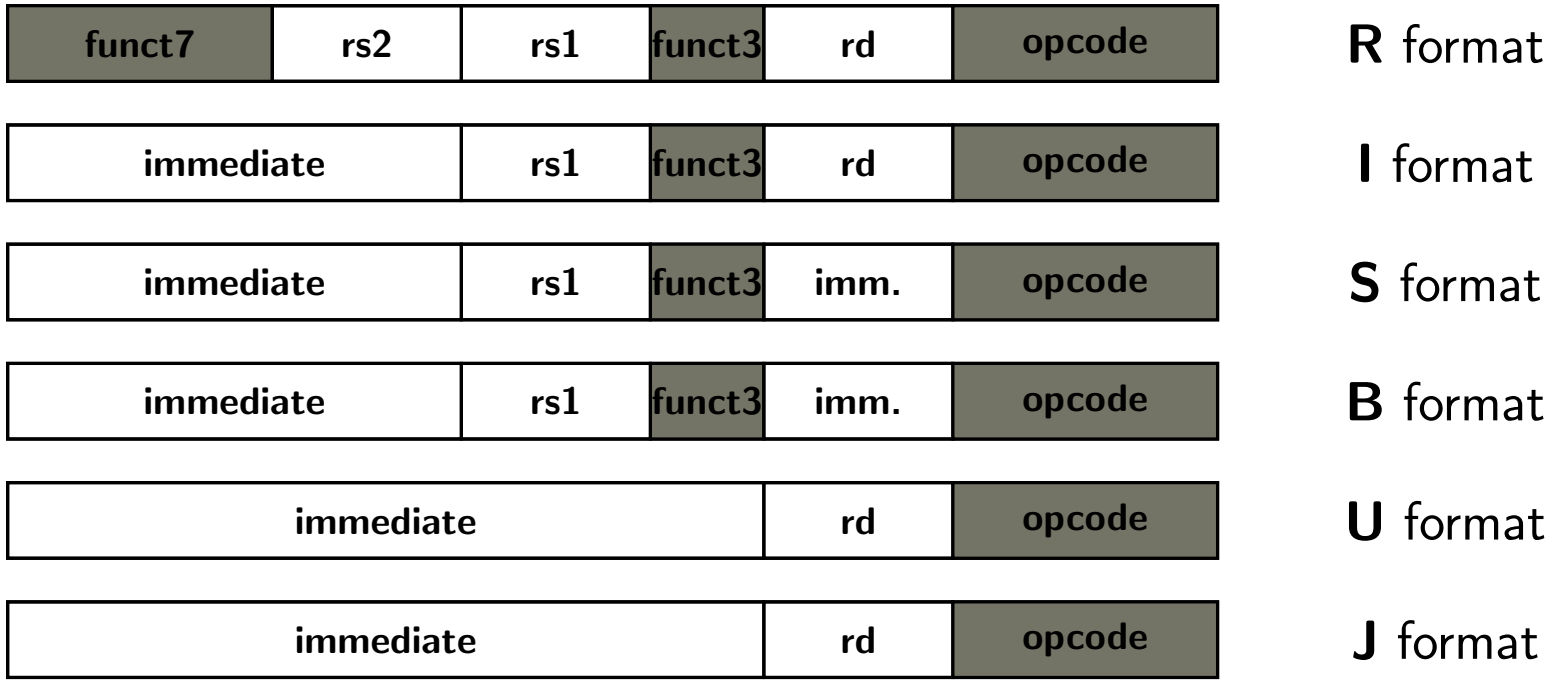

Differences between I/S/B and U/J in arrangement of bits throughout immediates: optimized to support hardware implementation

Instruction Anatomy in RISC-V®

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Formats/instruction coding are optimized for hardware design

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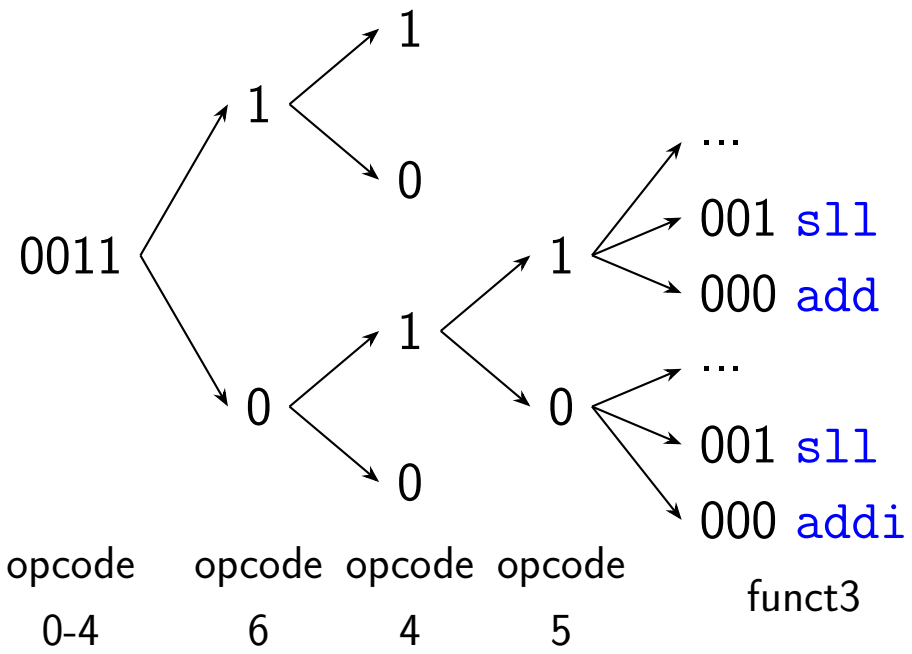

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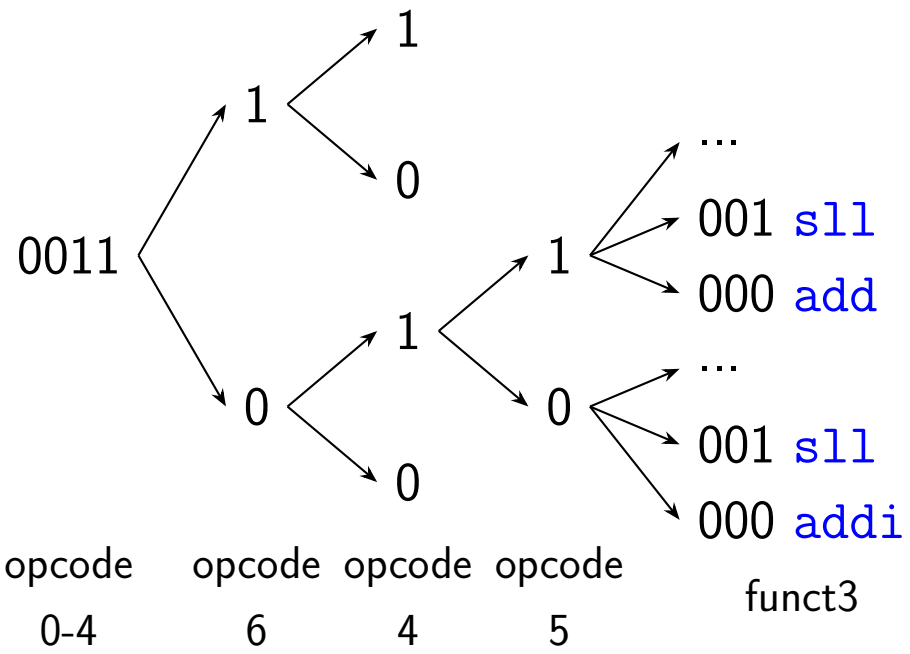

The opcode and function bits can be used to directly drive control lines (multiplexers, etc.)

APPLICATION BINARY INTERFACE

Example: RISC-V®

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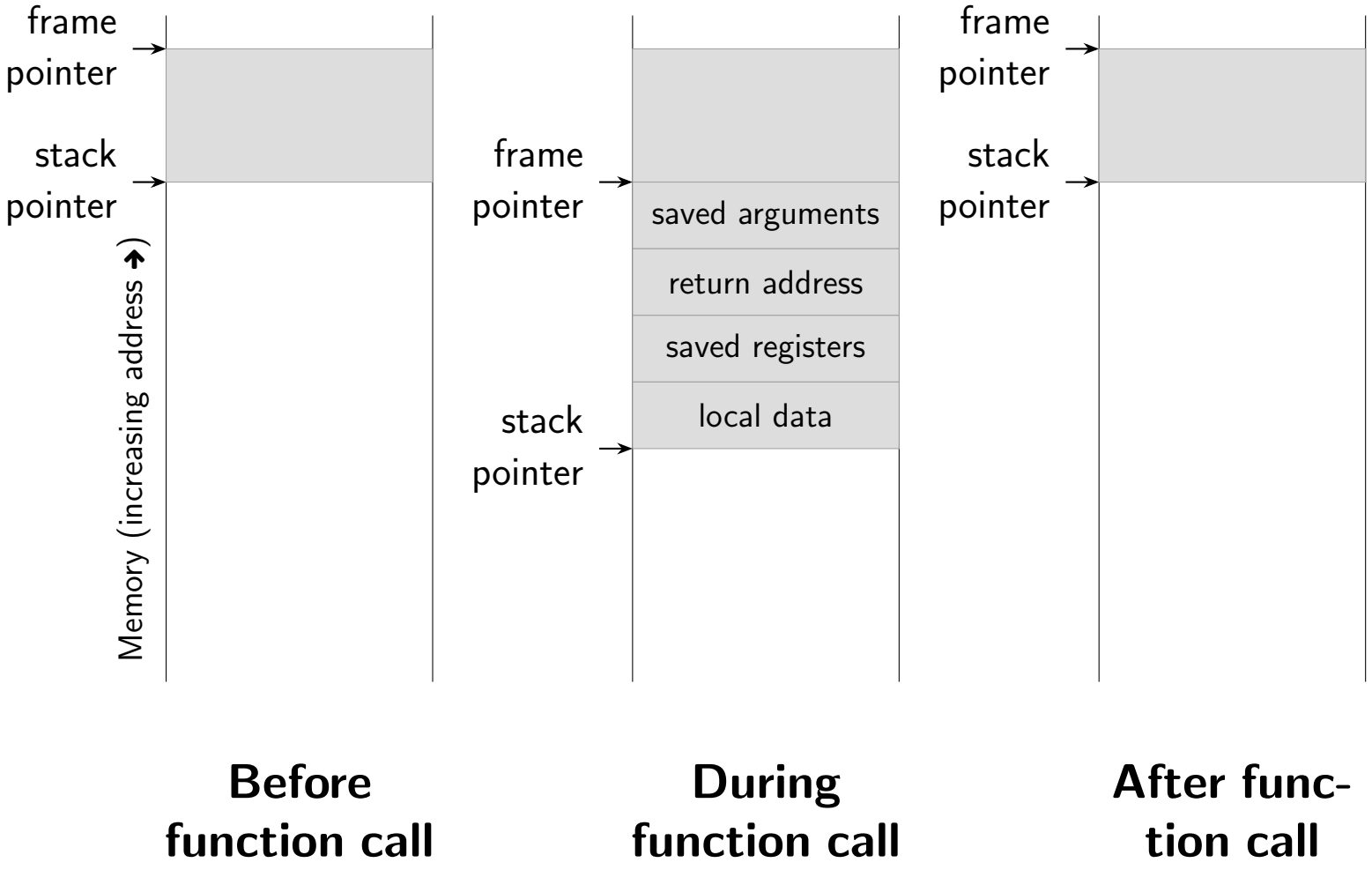
ABI adds **semantics** to instructions that is reflected in register "ABI names"
Examples in RISC-V: `a0` for `x10` as argument register, `t0` for `x5` as temporary, `zero` for `x0`, see chapter 25 in ISA spec

Stack Frame


frame pointer
stack pointer
Memory (increasing address ➔)
frame pointer
saved arguments
return address
saved registers
local data
stack pointer
frame pointer
stack pointer
Before function call
During function call
After function call

Calling Conventions

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Specified per ISA

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- Which registers are saved by the caller or the callee (RISC-V: see next)

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- Callee restores return address and executes `jalr` with it as target

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Some assembler programs (e.g., GNU AS in our lab) provide convenient use
For example: generic `add x2, x1, -2` as alias for `addi`

PRIVILEGE LEVELS AND EXCEPTIONS

Example: RISC-V®

Interaction with environment

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- Execution environments abstract from underlying hardware
- Potentially protects from malicious code controlling the system with **privileges**

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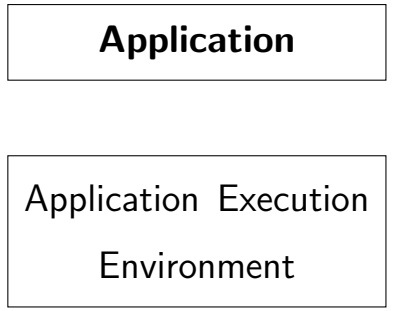

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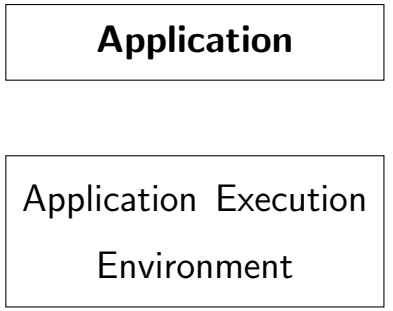

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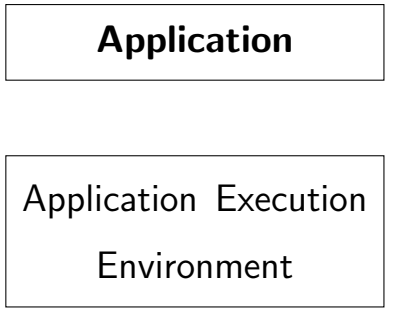

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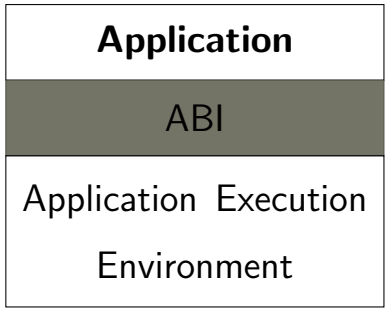

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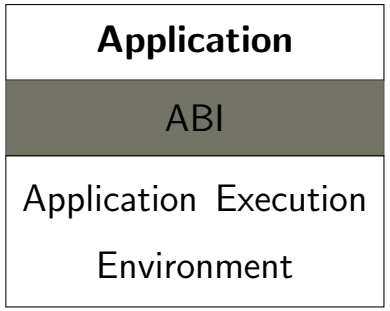

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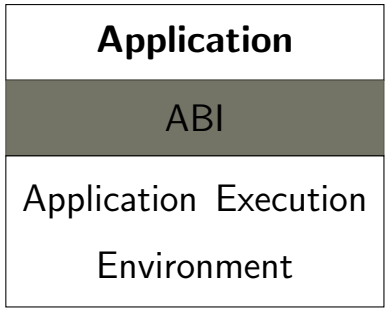

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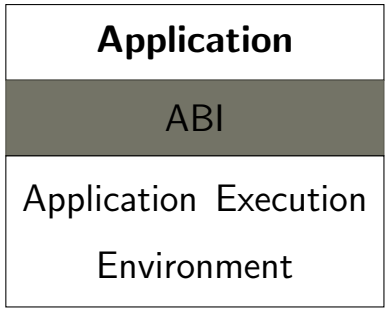
Very common AEE (also in our lab): simulators



Supervisor Privileges

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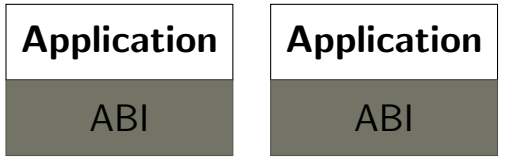
Extend AEE with multitasking



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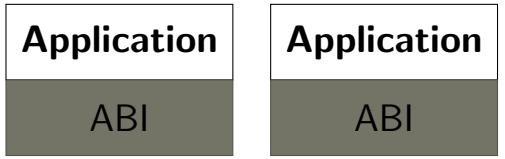

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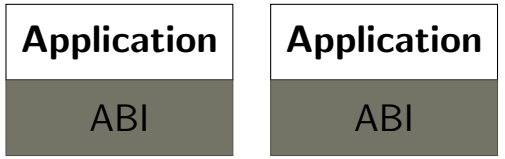

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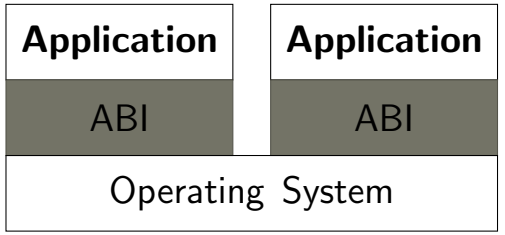

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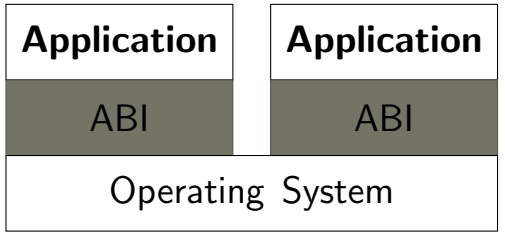

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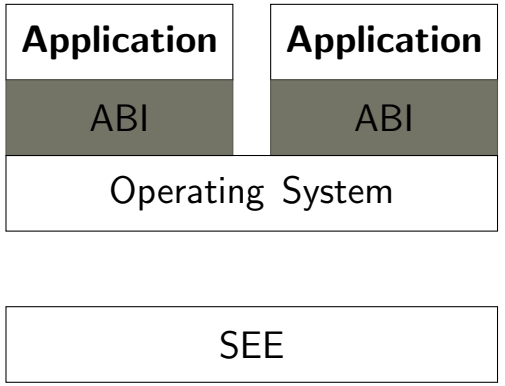

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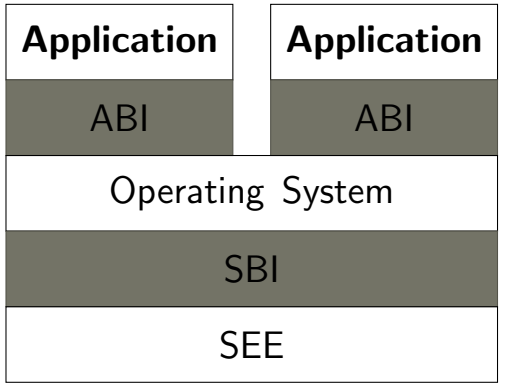

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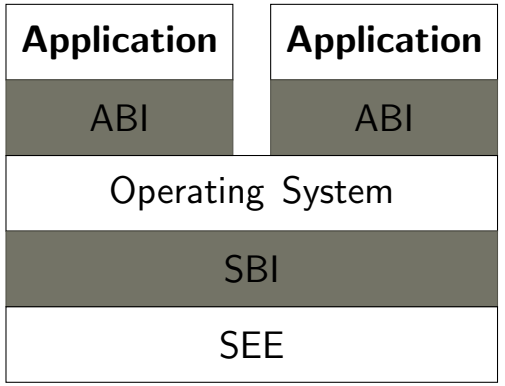
- Basic SEEs: BIOS-style IO system, boot loader



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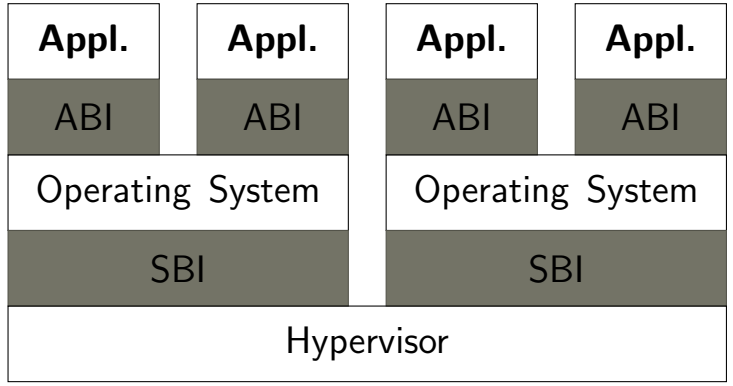

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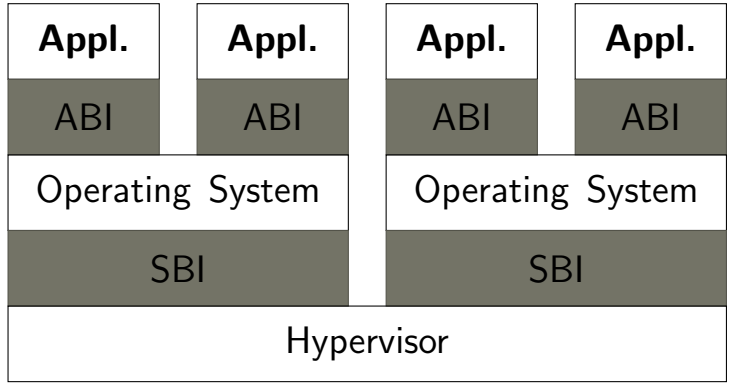

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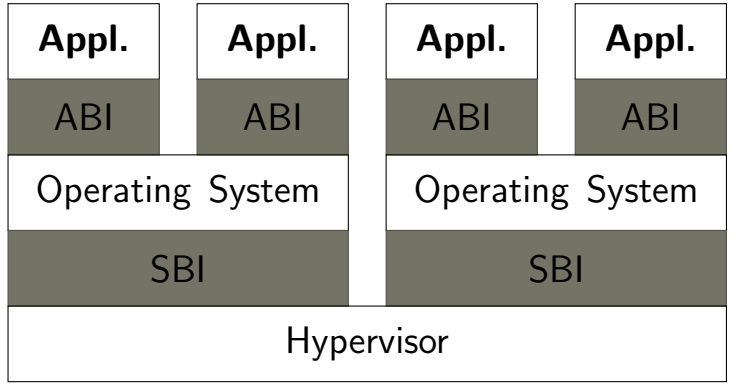

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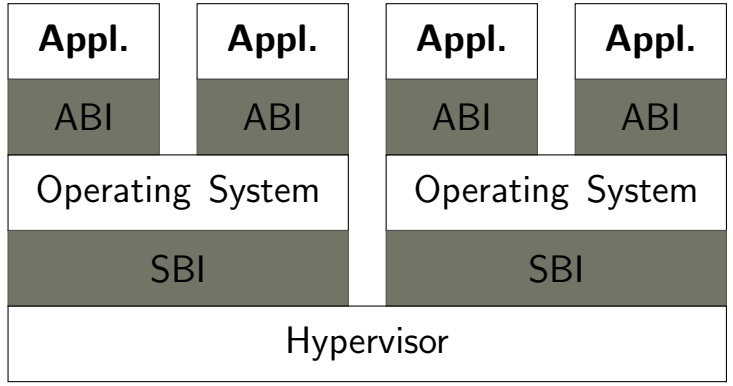

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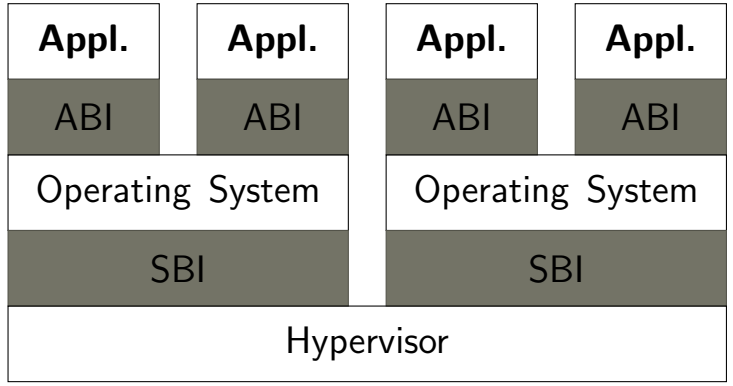

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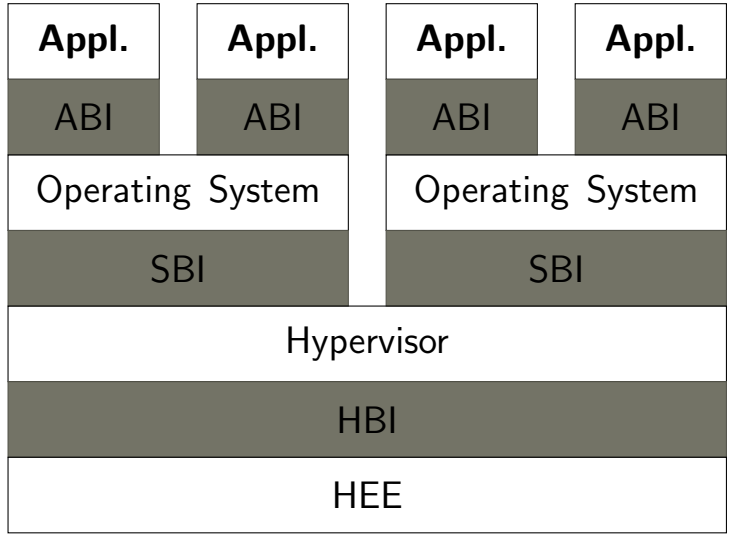

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- *Synchronous* exceptions: exceptions that relate to an instruction (divide by zero, page fault, etc.)

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- *Synchronous* exceptions: exceptions that relate to an instruction (divide by zero, page fault, etc.)
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Performance improvement: delegation

- Let "higher" modes handle exceptions
- Delegation reduces overhead of switching, typical example: Let guest OS in virtualization directly handle page fault and not fault to machine mode

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- Generic model of a processor
- Difference between ISA and Microarchitecture
- RISC vs. CISC
- Basic instruction set architecture, example RISC-V