Fakultät für
Informatik und
Mathematik

HOCHSCHULE
FÜR ANGEWANDTE
WISSENSCHAFTEN
MÜNCHEN

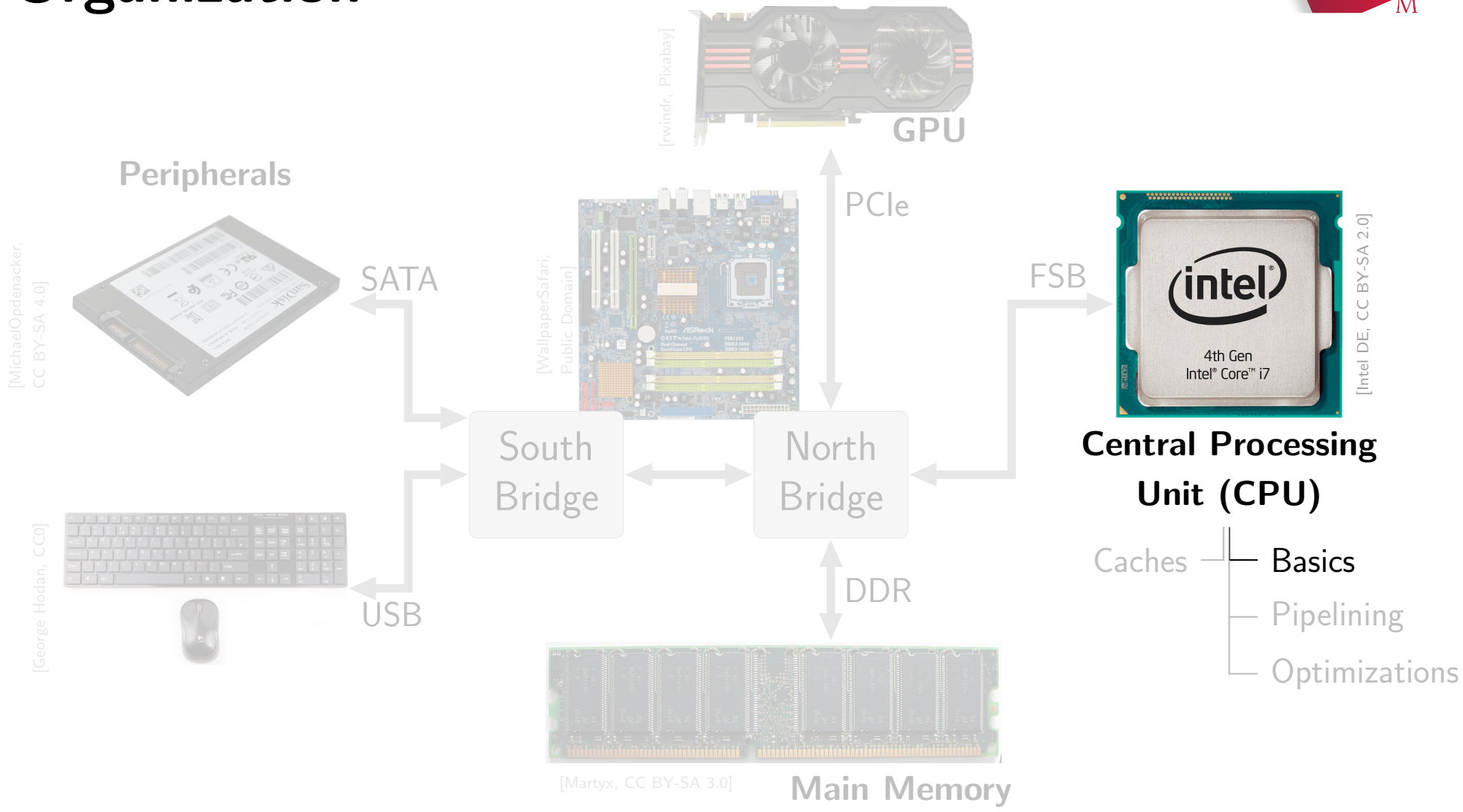
COMPUTER ARCHITECTURE

Chapter 3 – CPU Pipelining

Prof. Dr.-Ing. Stefan Wallentowitz

Department 07 – Munich University of Applied Sciences

Course Organization



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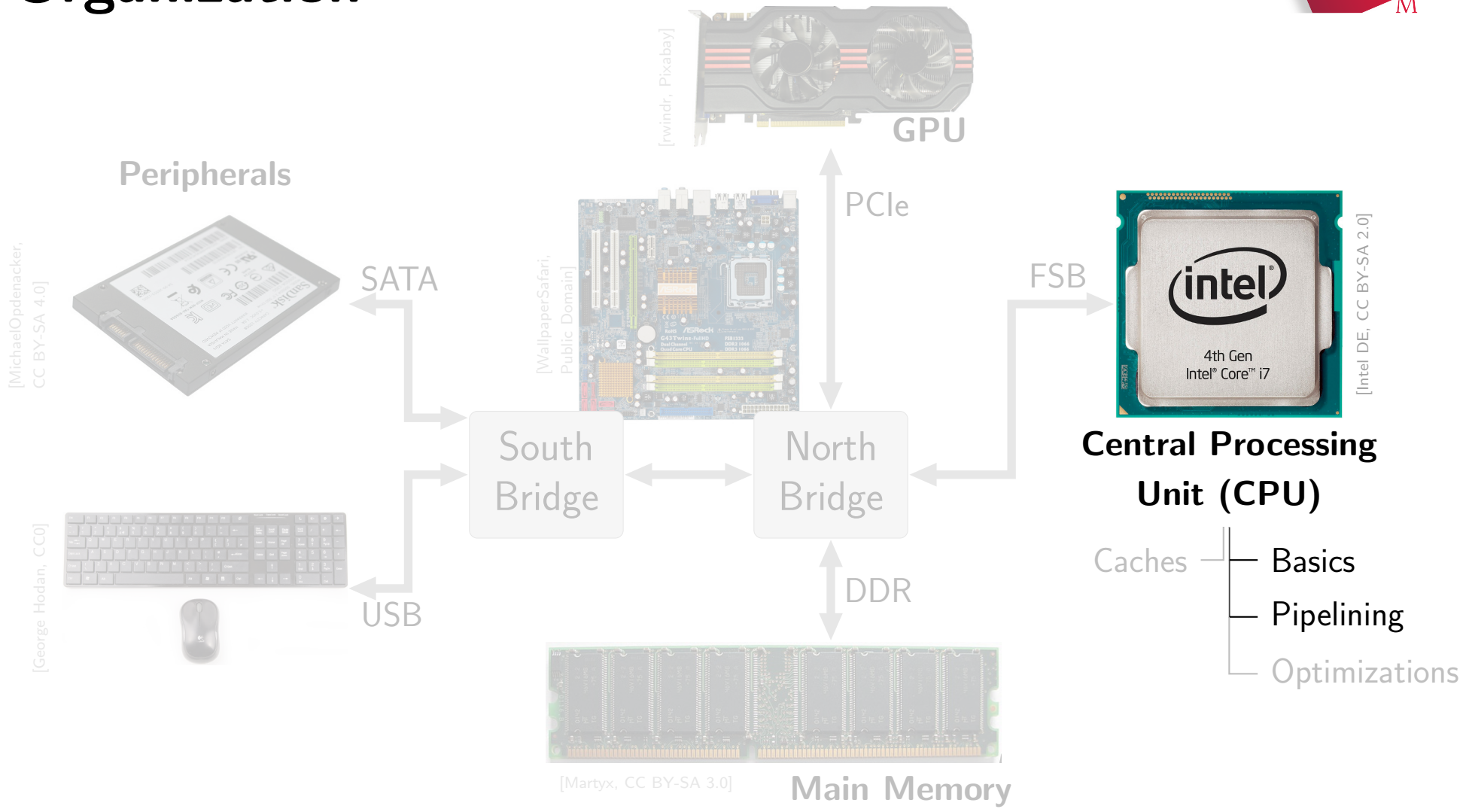
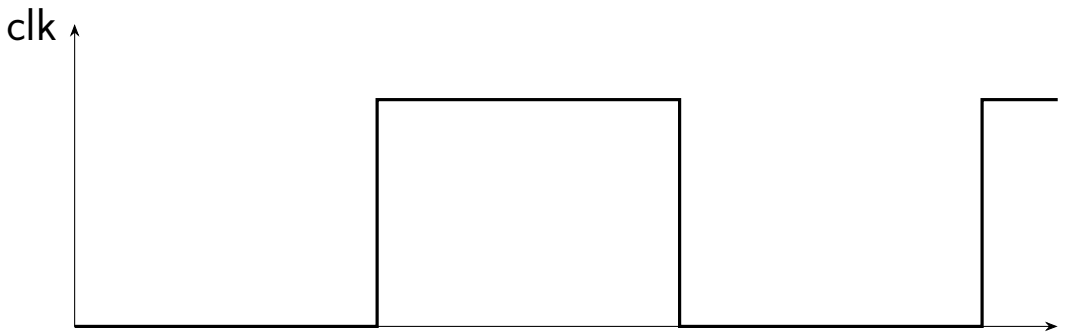


Recap: Instruction Processing



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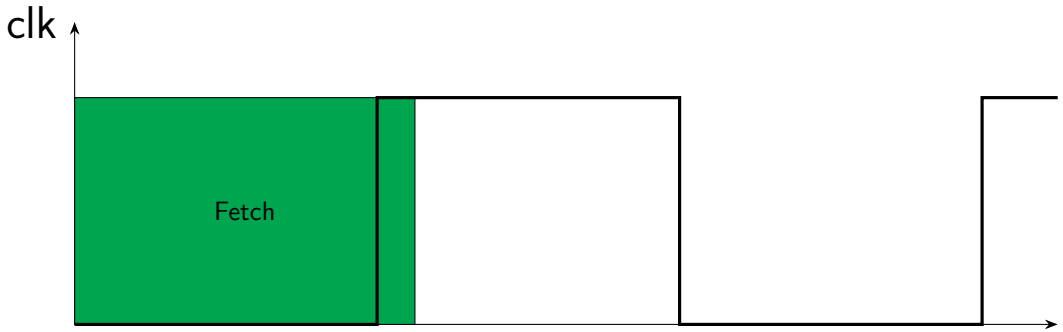
Fetch instruction (short: FE)



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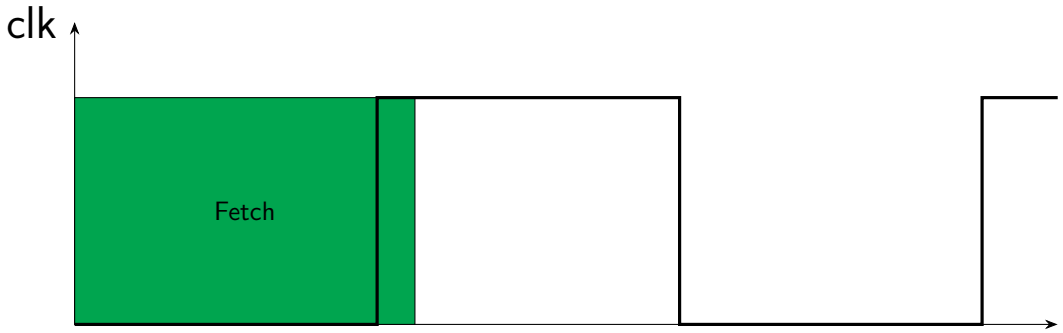

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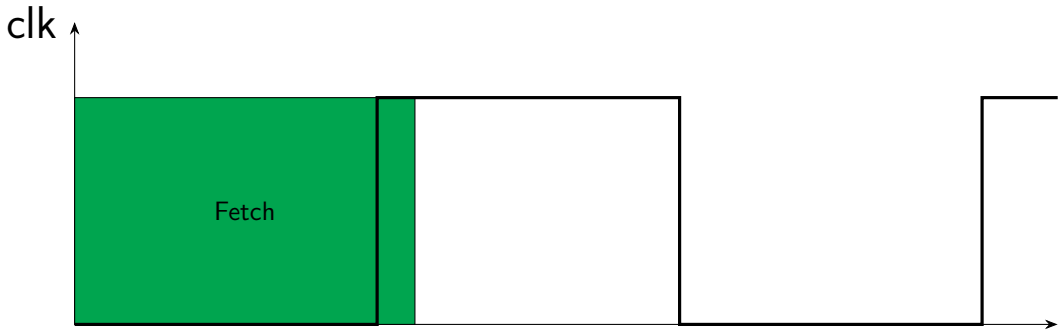
Fetch instruction (short: FE)

- Pointer to next instruction from current program counter
- Load the instruction from memory



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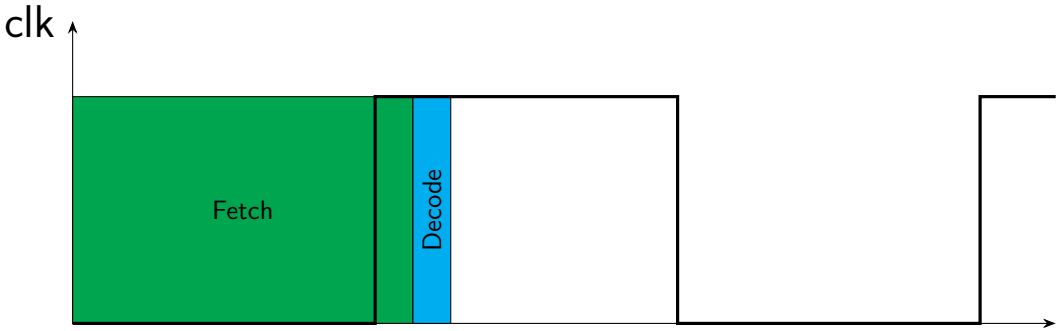

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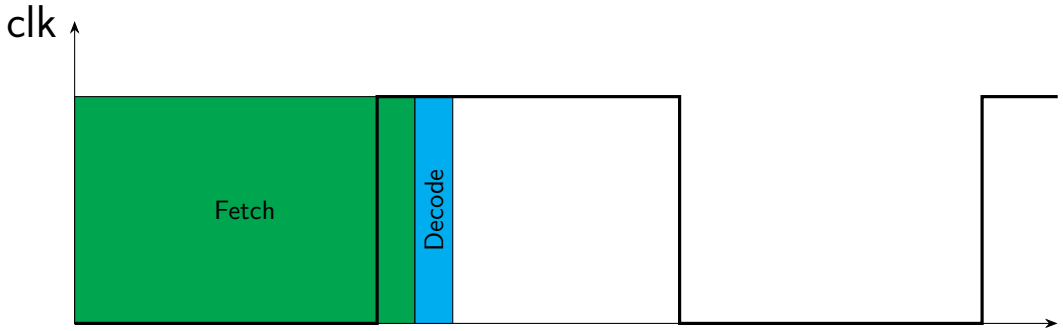

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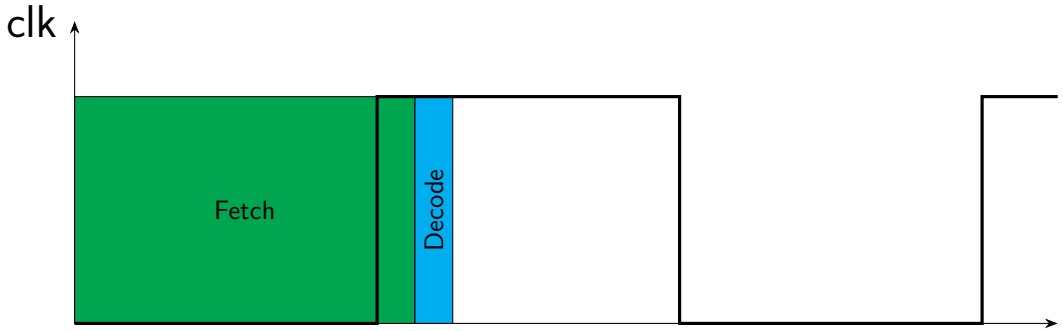

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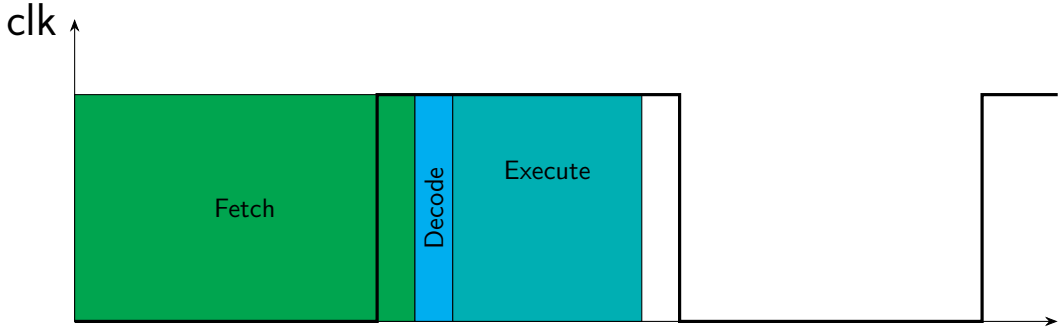

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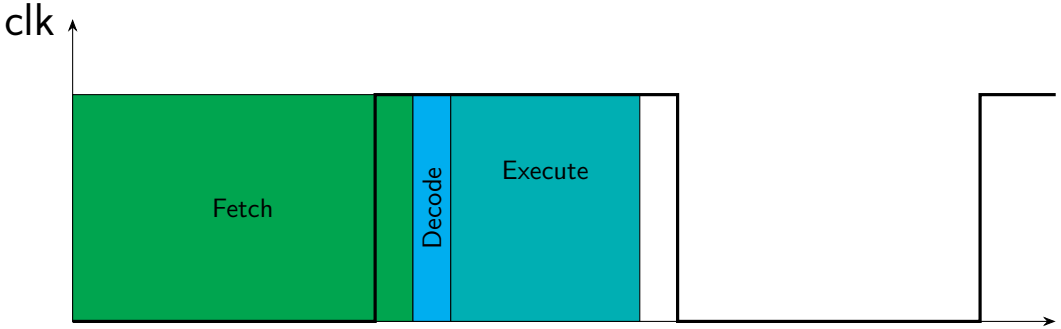

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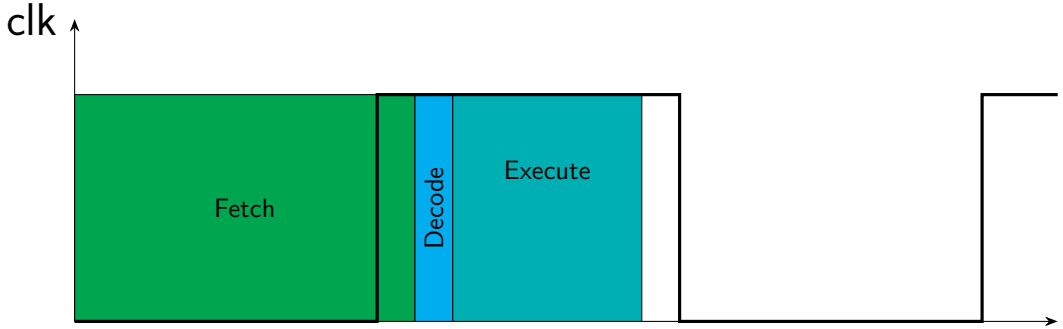

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Execute (EX)

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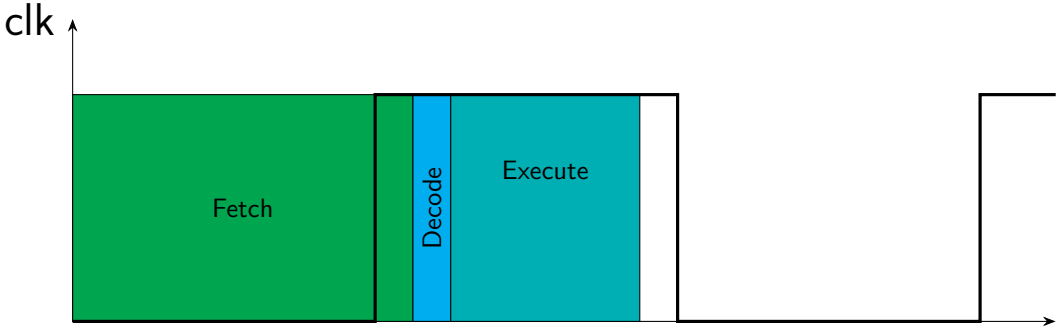
- Calculate effective address
- Control flow: check condition



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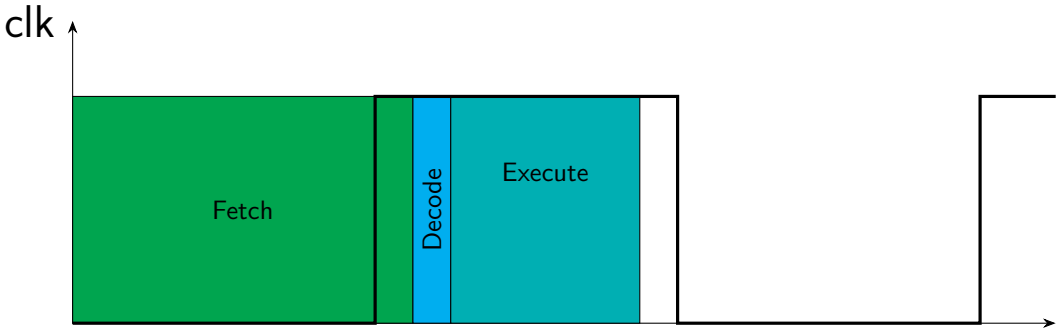
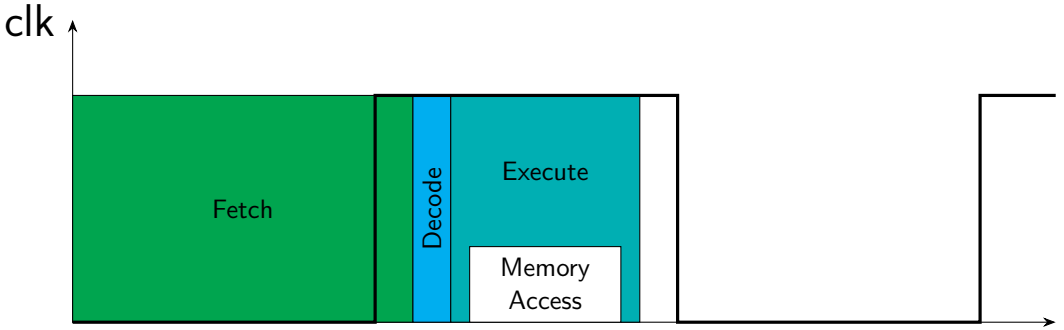


Recap: Instruction Processing

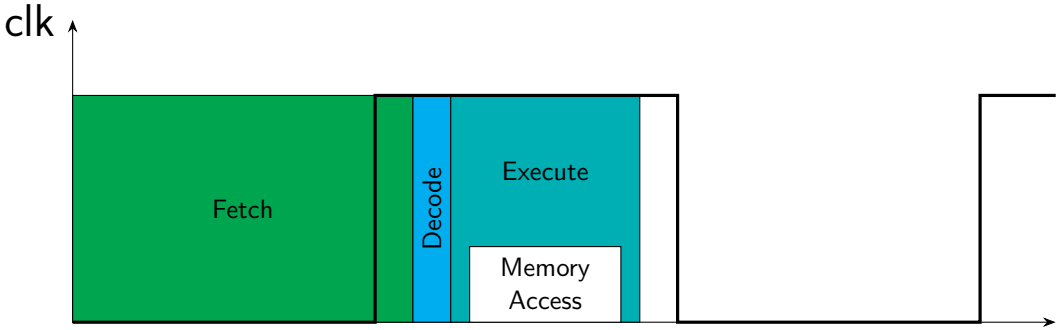
Memory Access (MA)



Recap: Instruction Processing

Memory Access (MA)

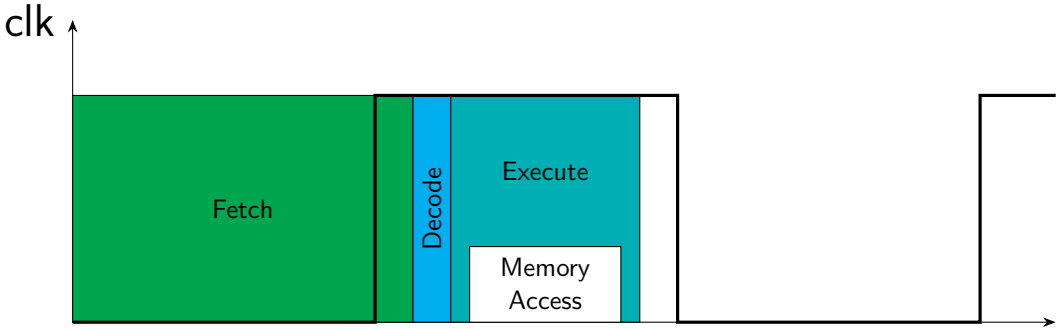
- Reading or writing to memory



Recap: Instruction Processing

Memory Access (MA)

- Reading or writing to memory
- optional



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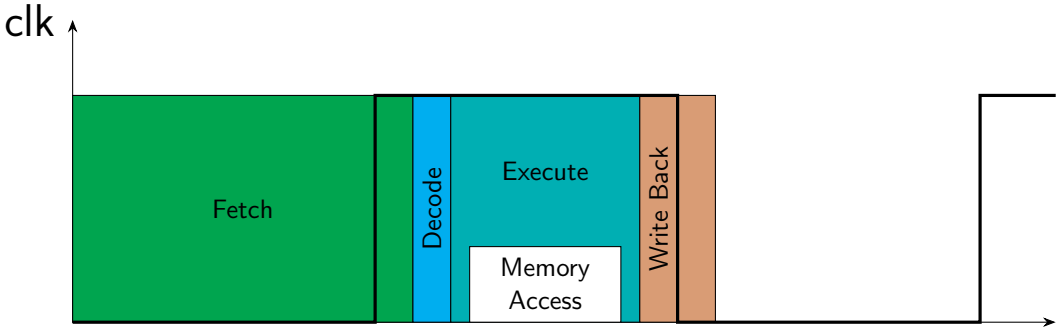
Write Back (WB)



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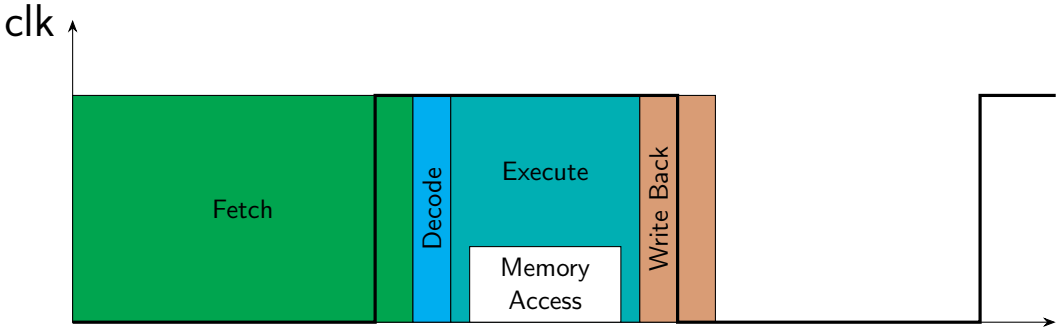

Recap: Instruction Processing

Memory Access (MA)

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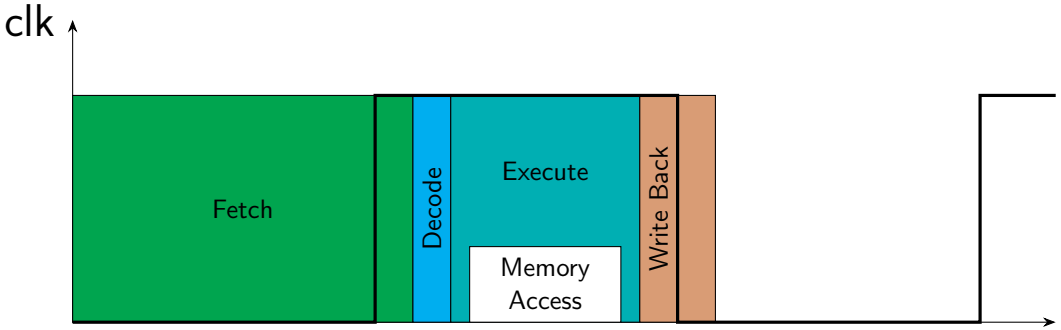
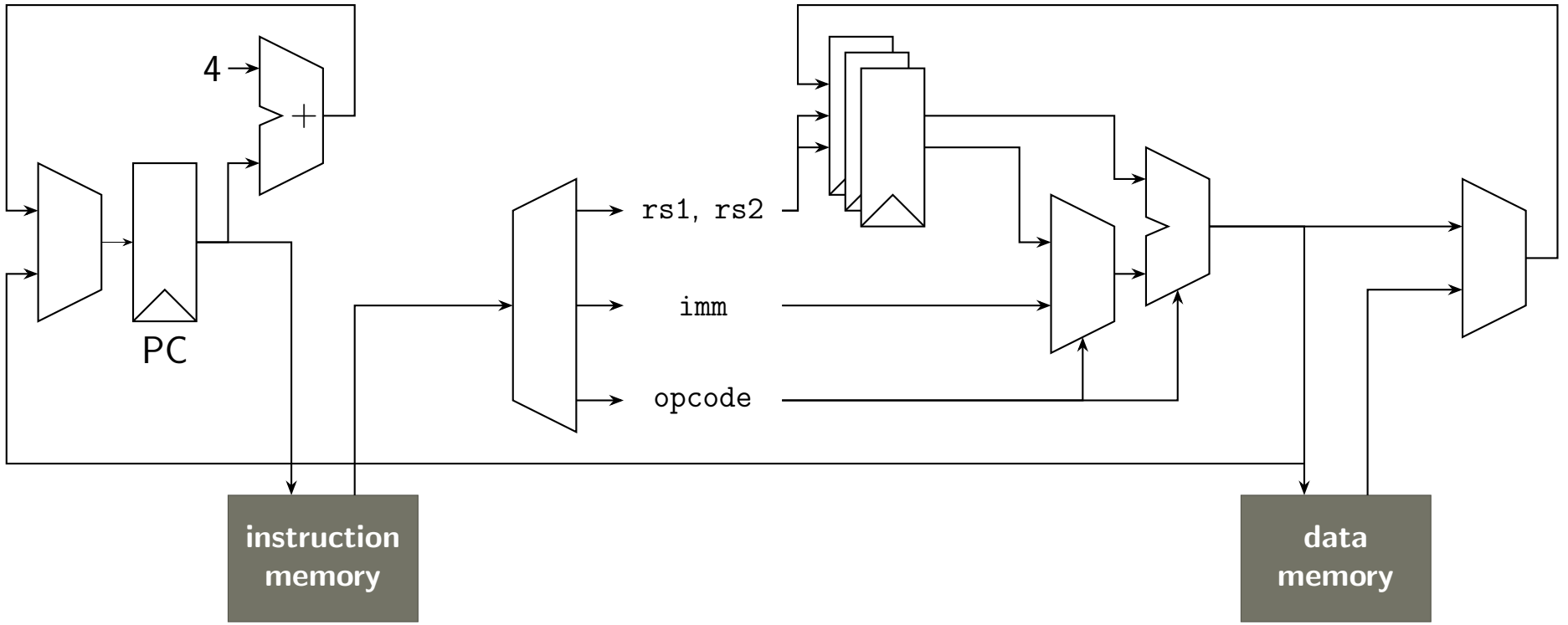
Write Back (WB)

- Write result into destination register
- Commit new program counter



Hardware Implementation (simplified)



Serial Execution

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slli x1, x2, 4
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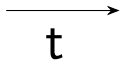

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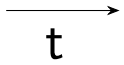
FE



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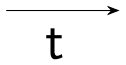

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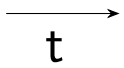

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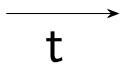

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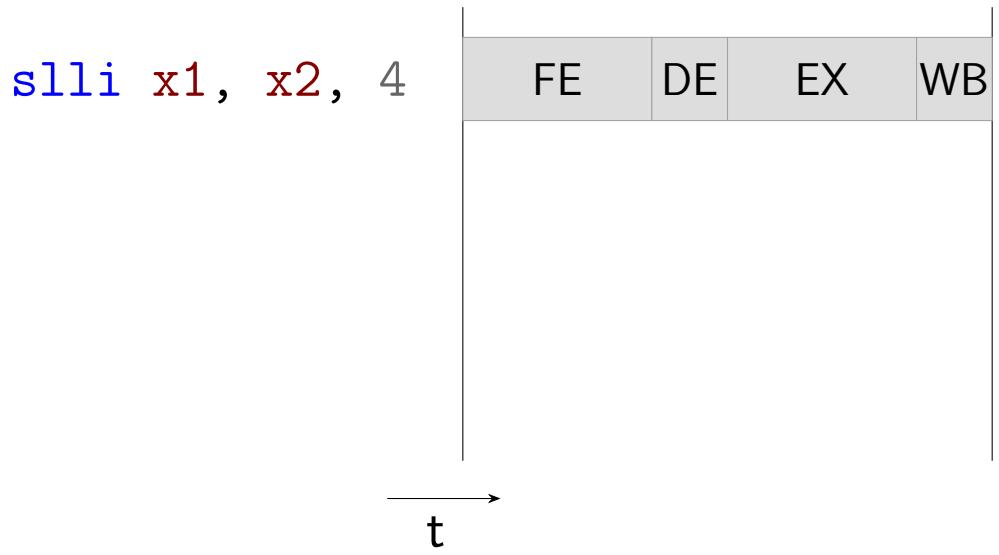

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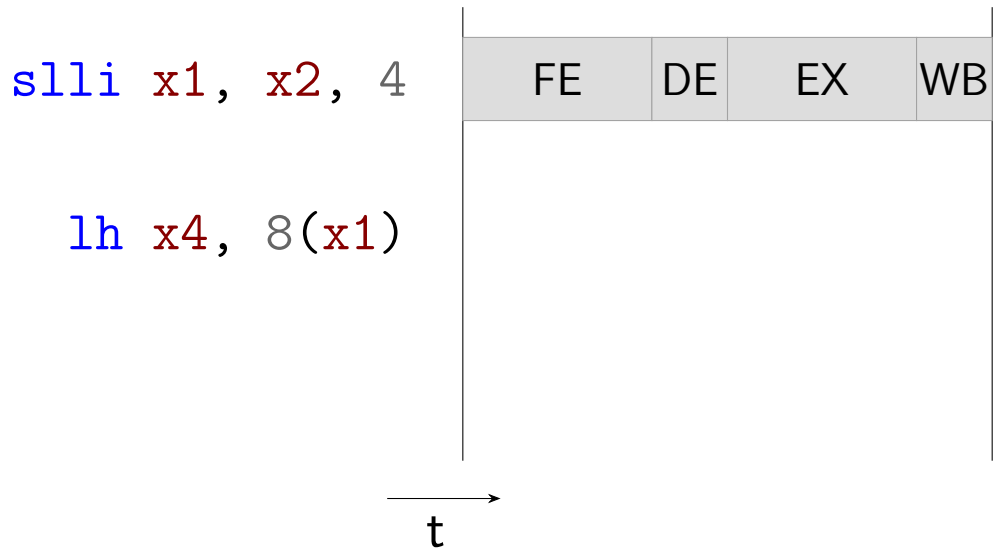

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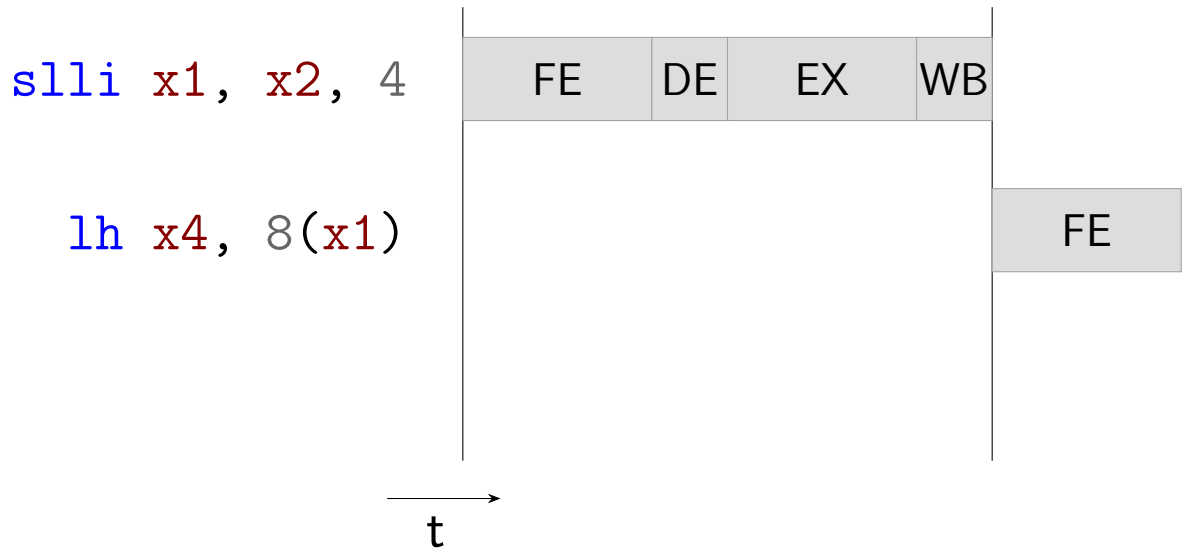

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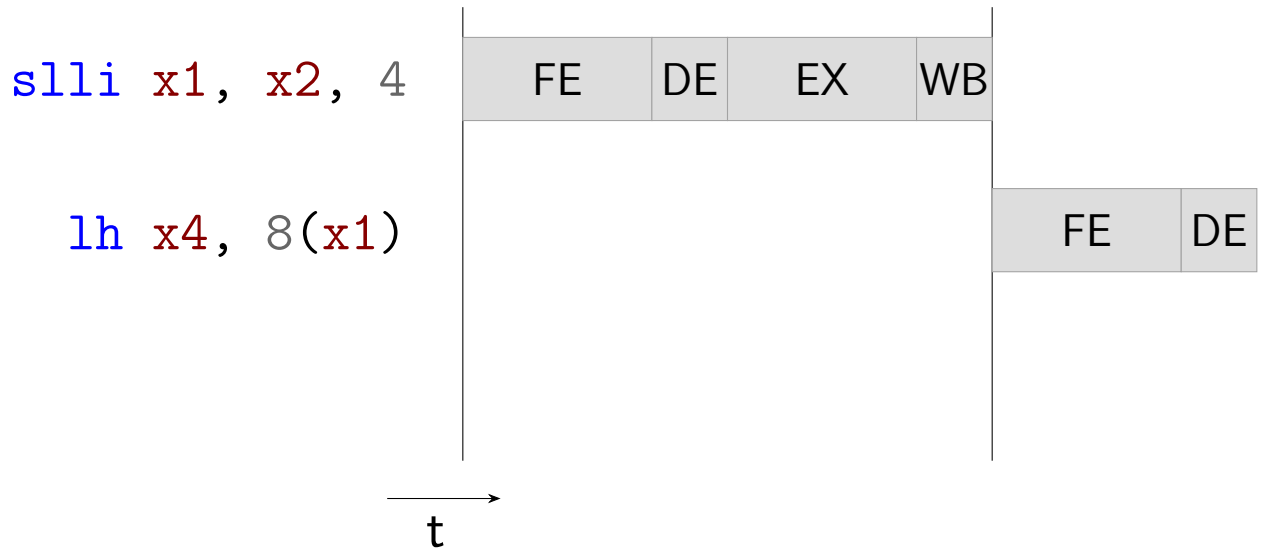

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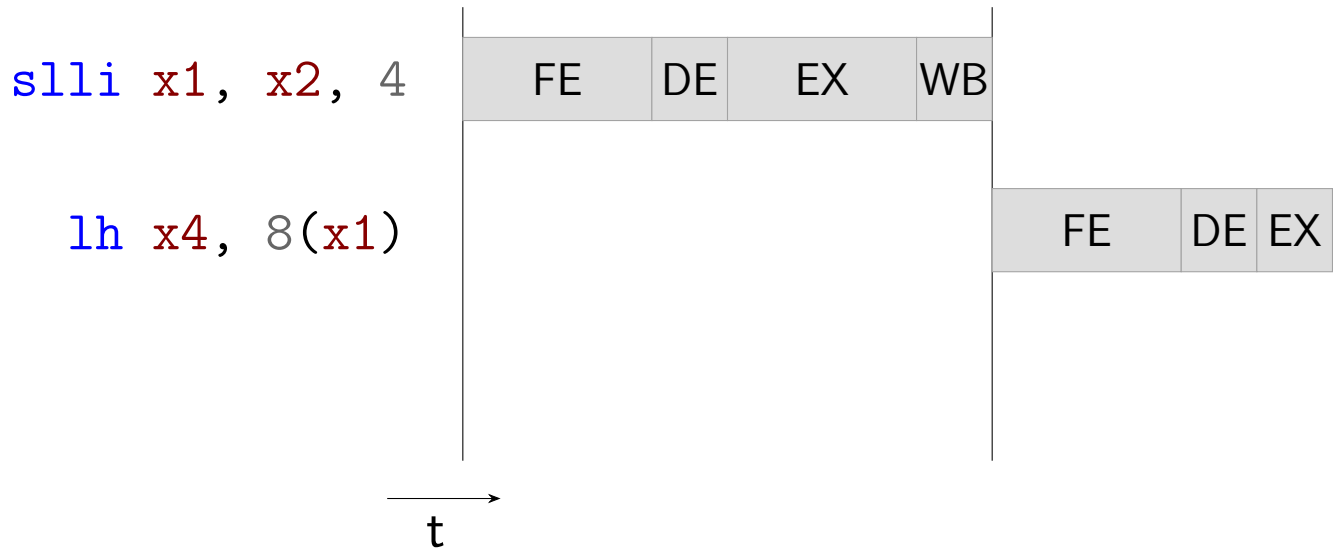

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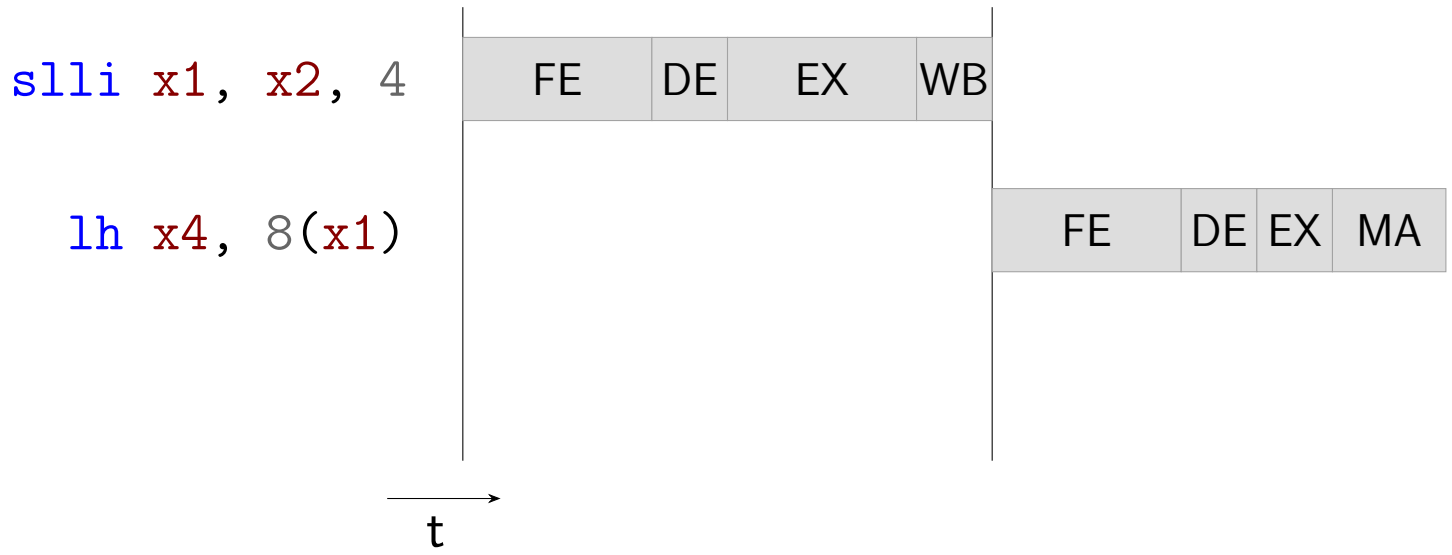

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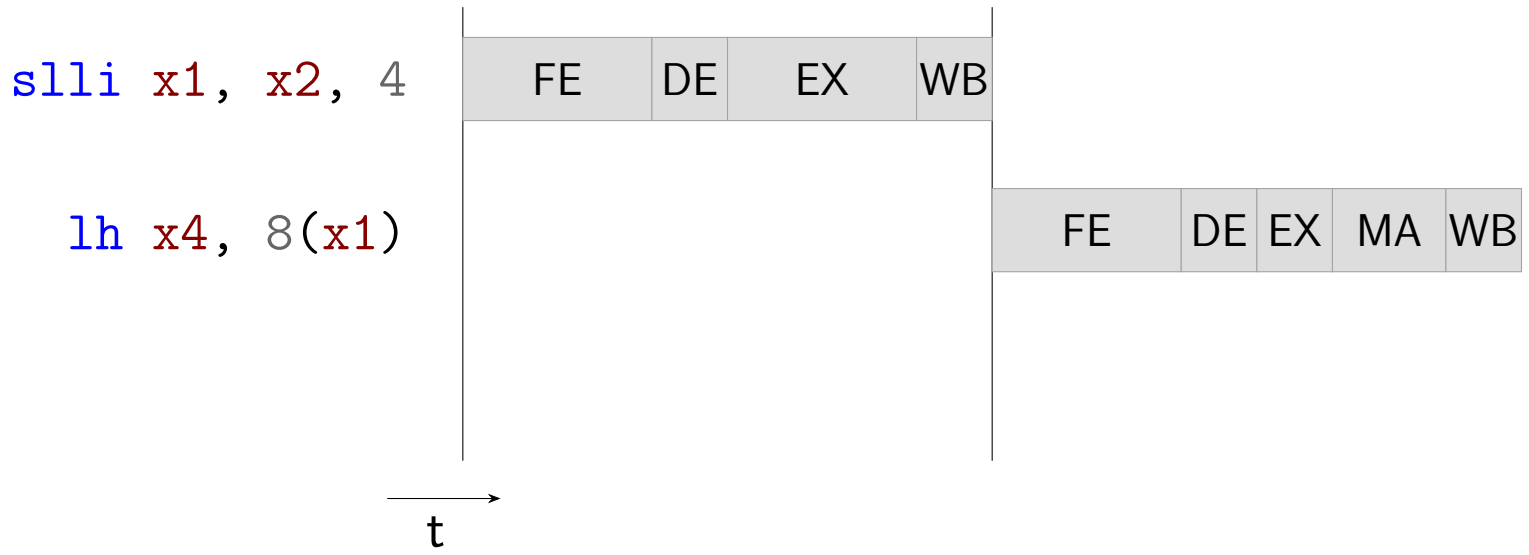

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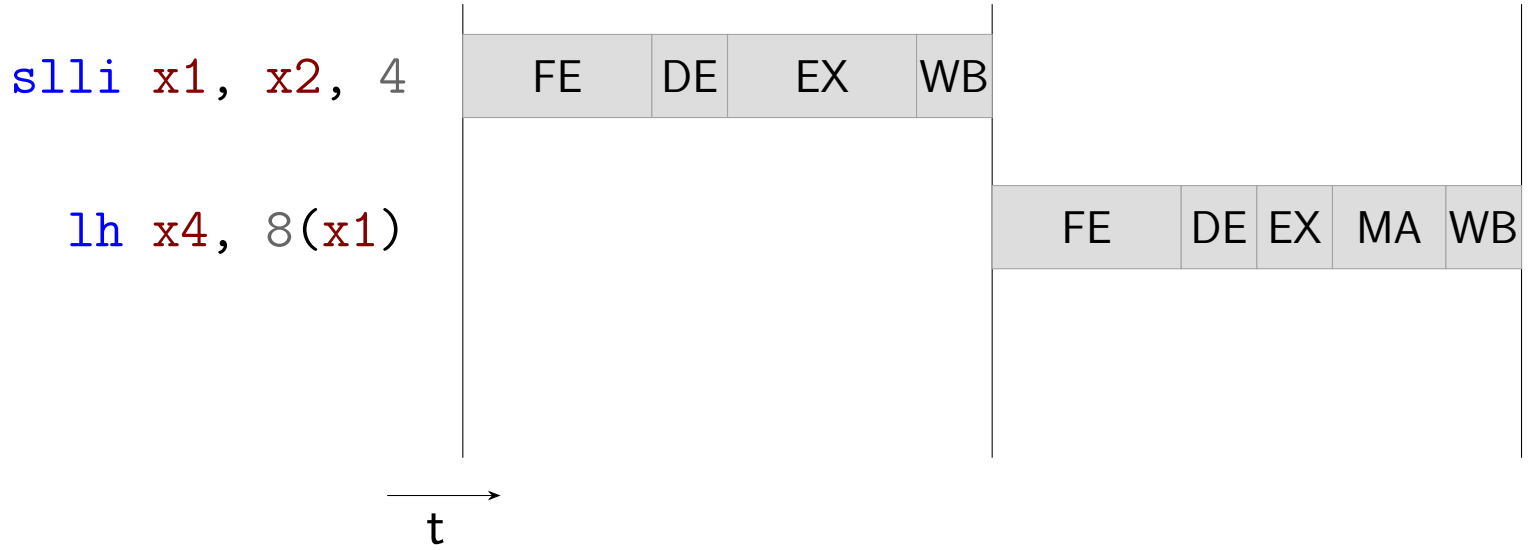

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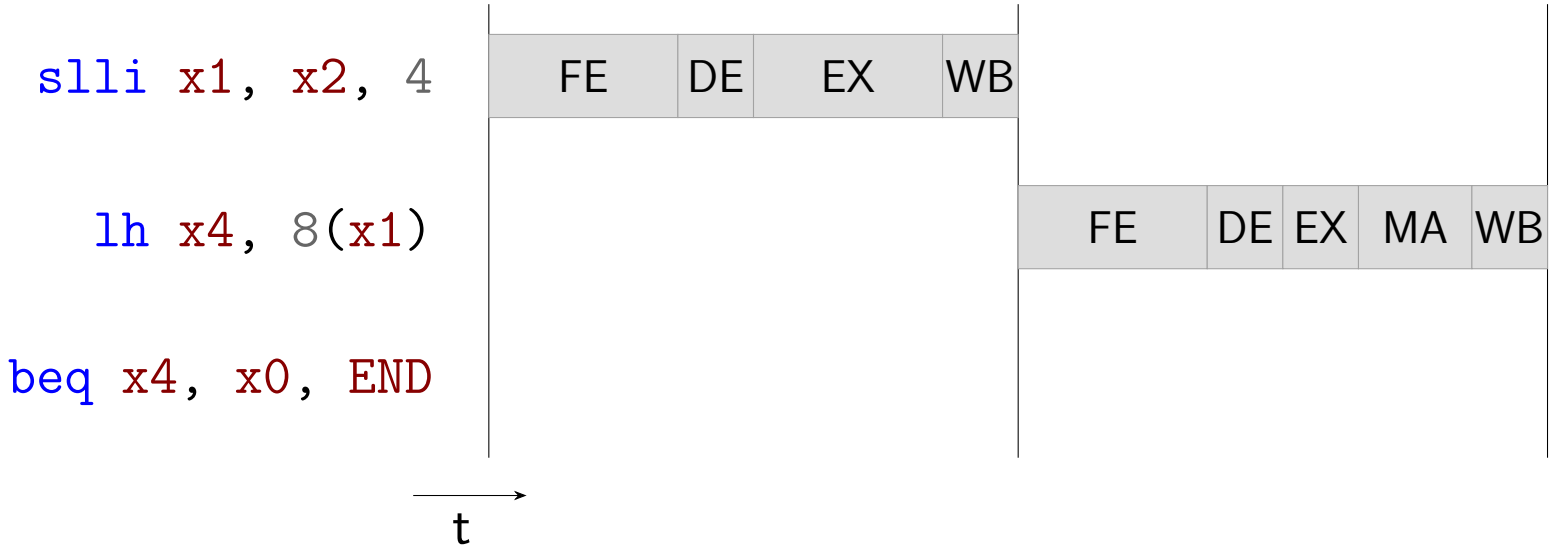

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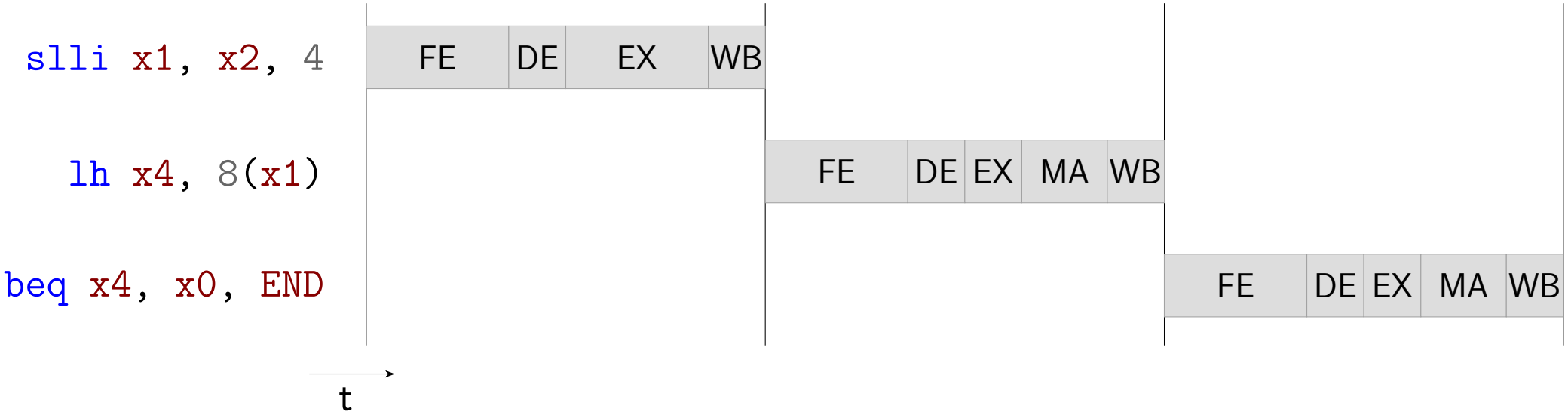

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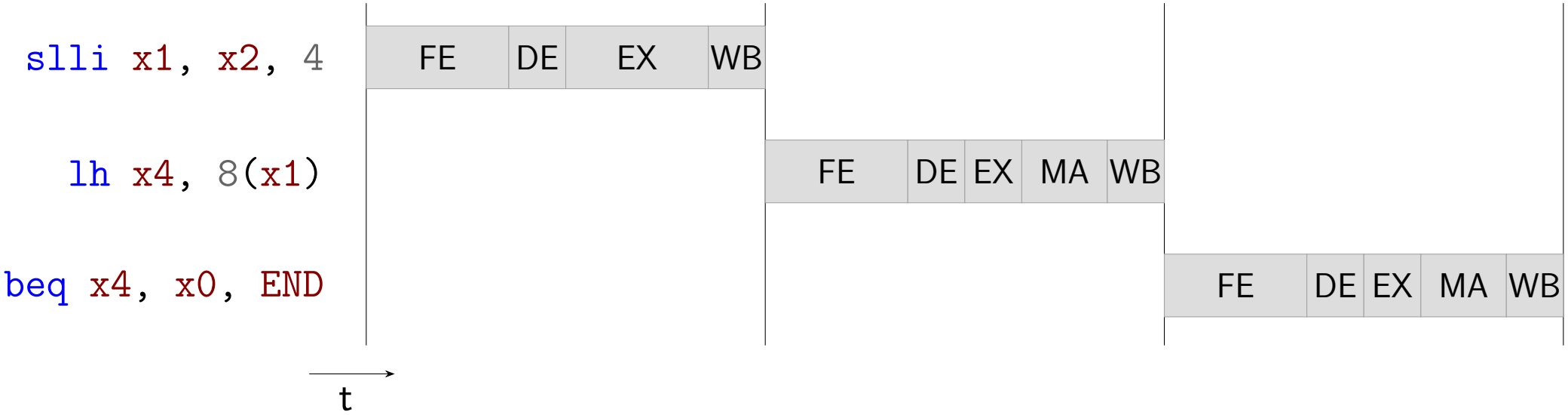

Can this be executed more efficiently?

Inspiration: Assembly Line

(c) BlueSpringsFordParts, CC BY 2.0

Instruction Pipelining

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Overlapping execution of instructions

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- Start phase for next instruction once current completes phase

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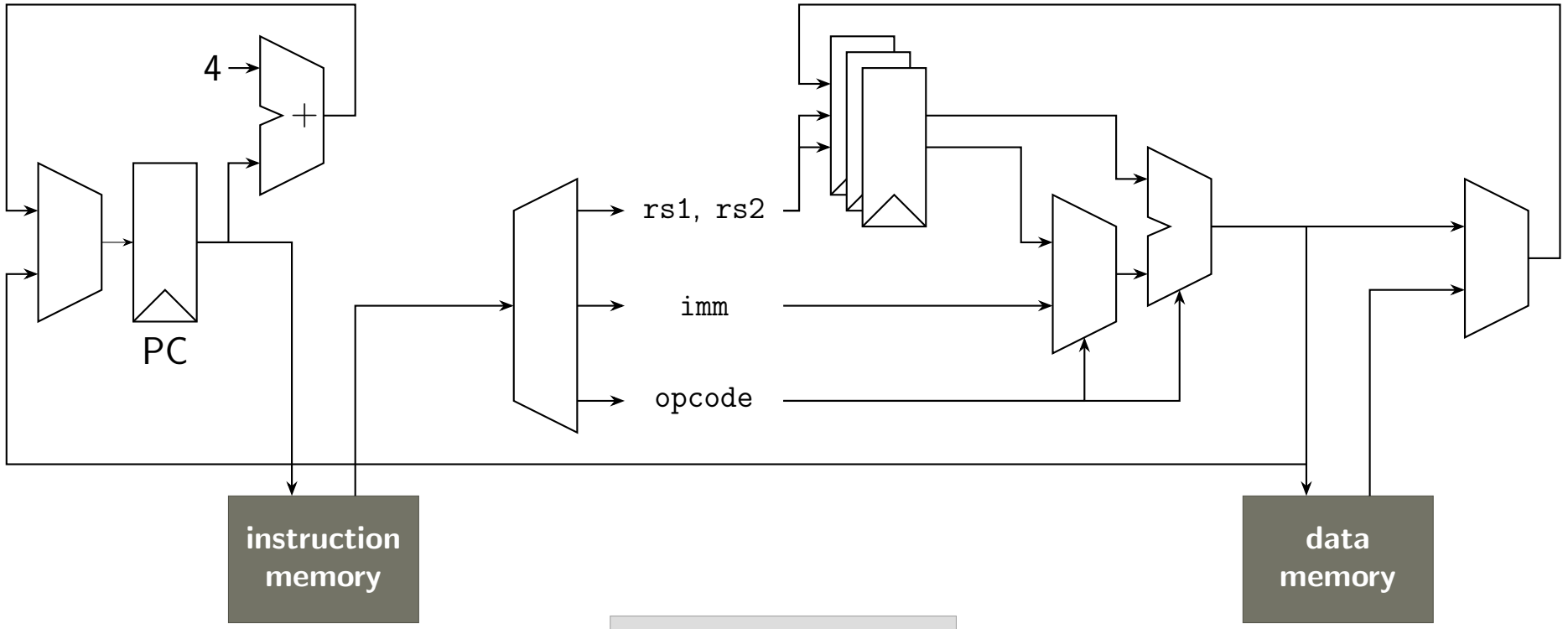
Key technology for fast CPU implementations

Hardware Implementation (simplified)



Where are the pipeline stages?

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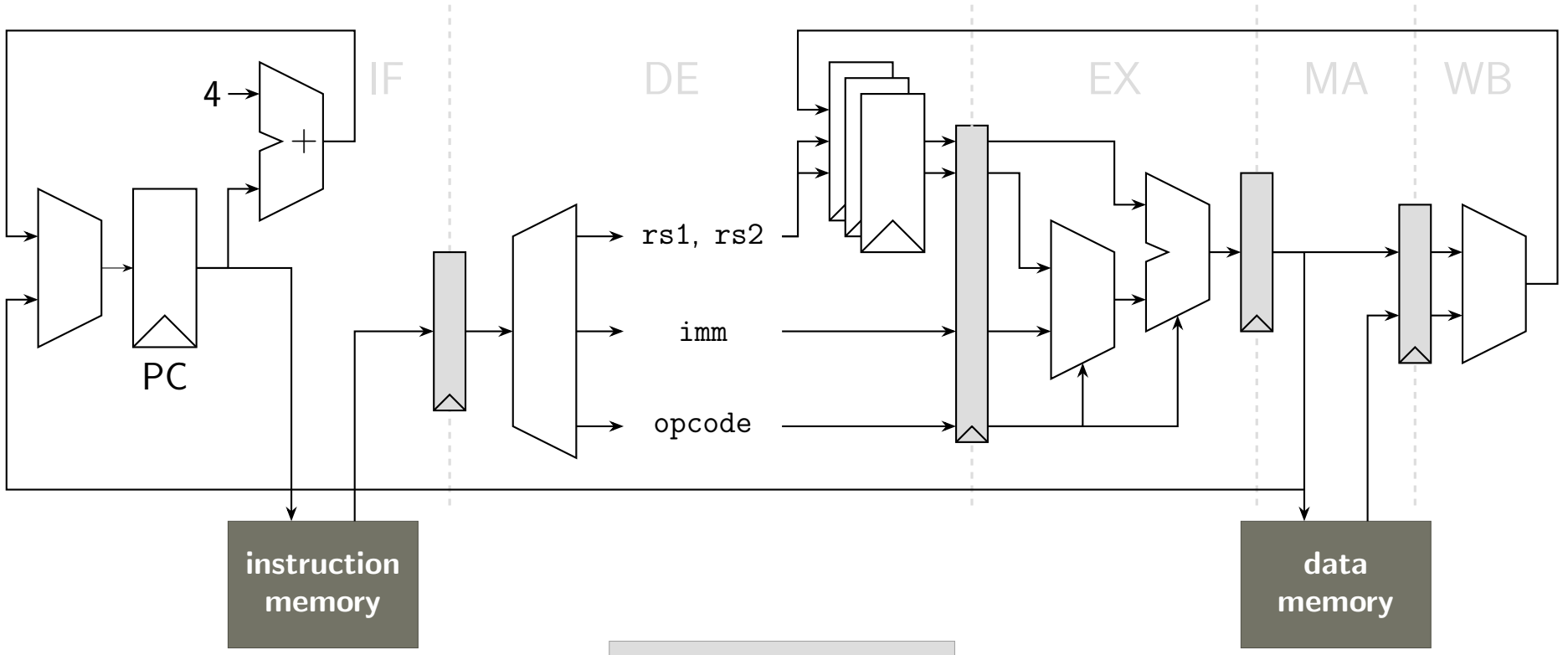

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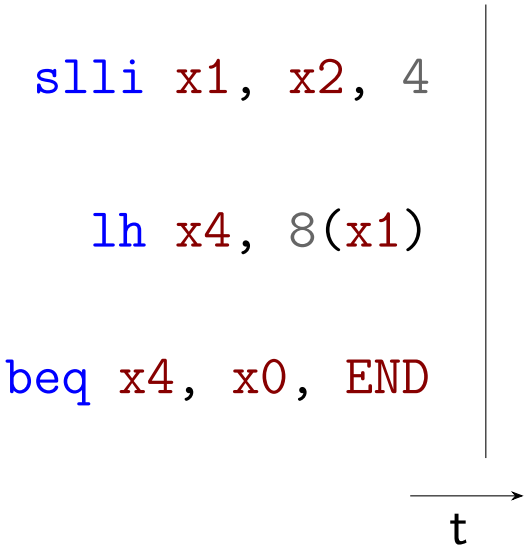
Pipeline Speedup



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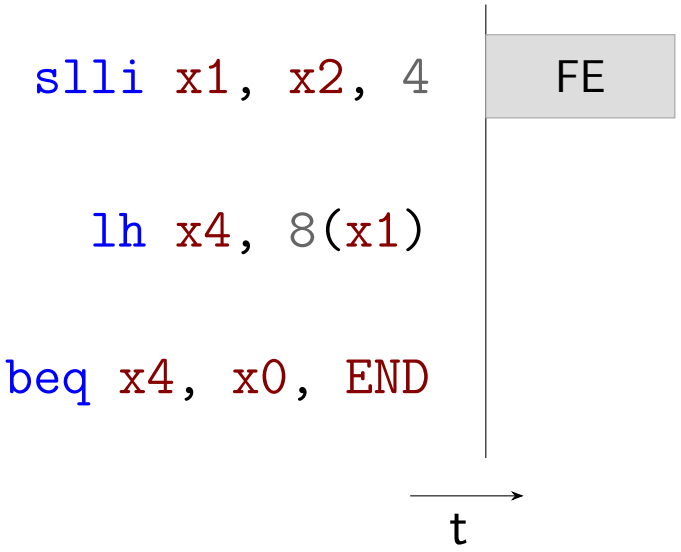
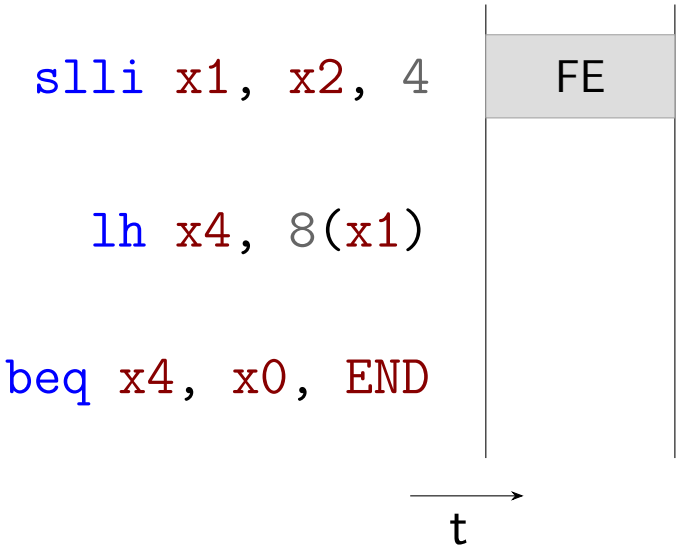


Pipeline Speedup



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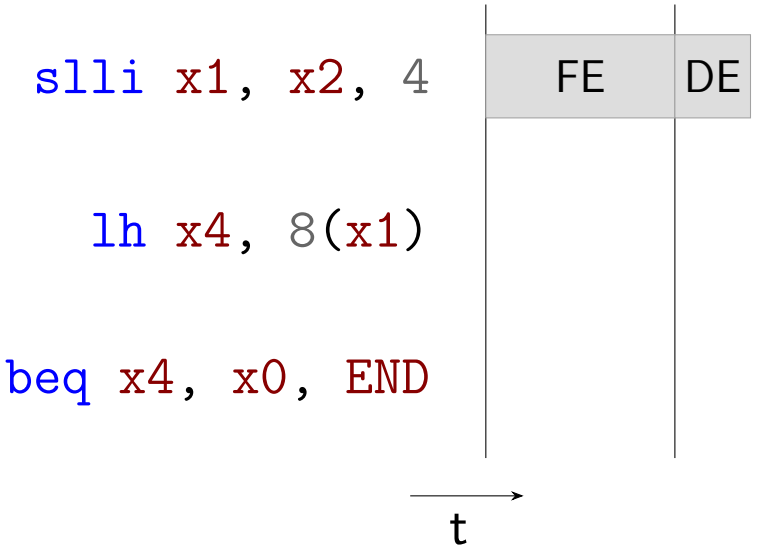

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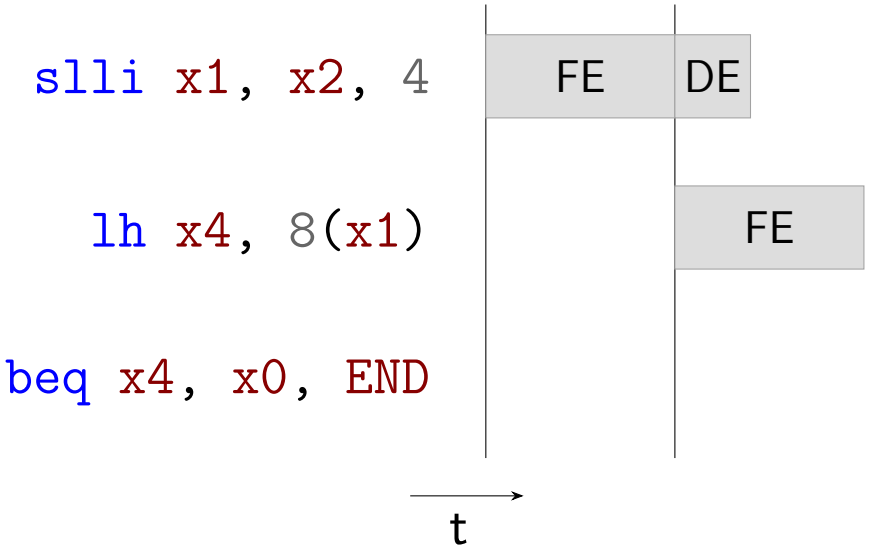

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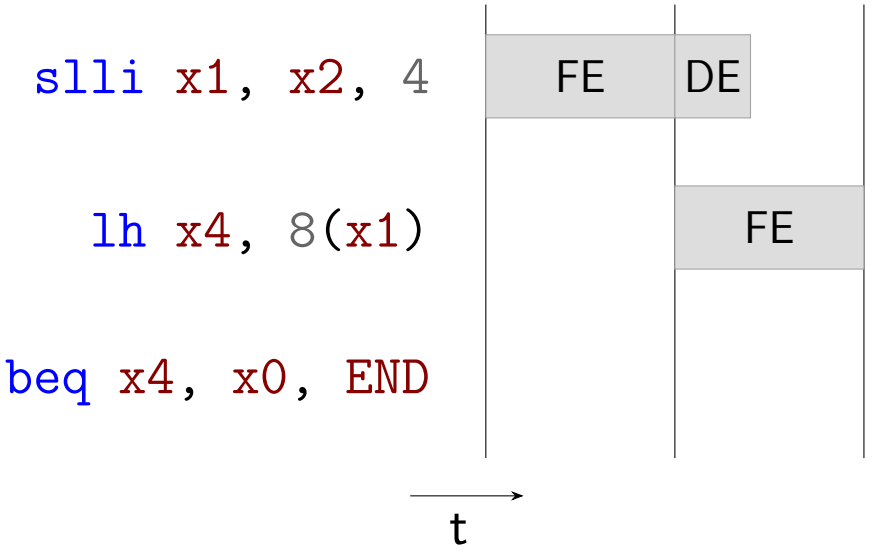

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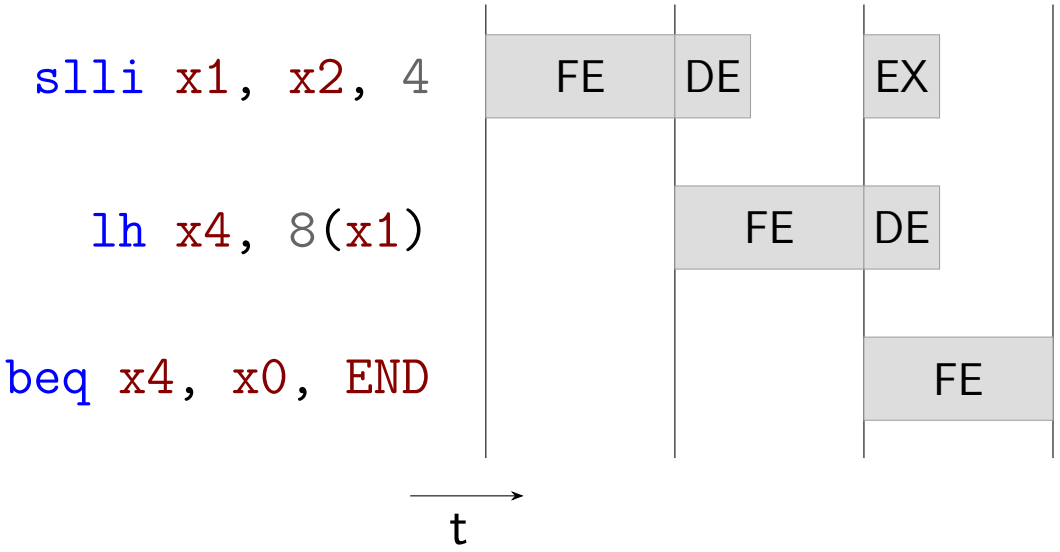

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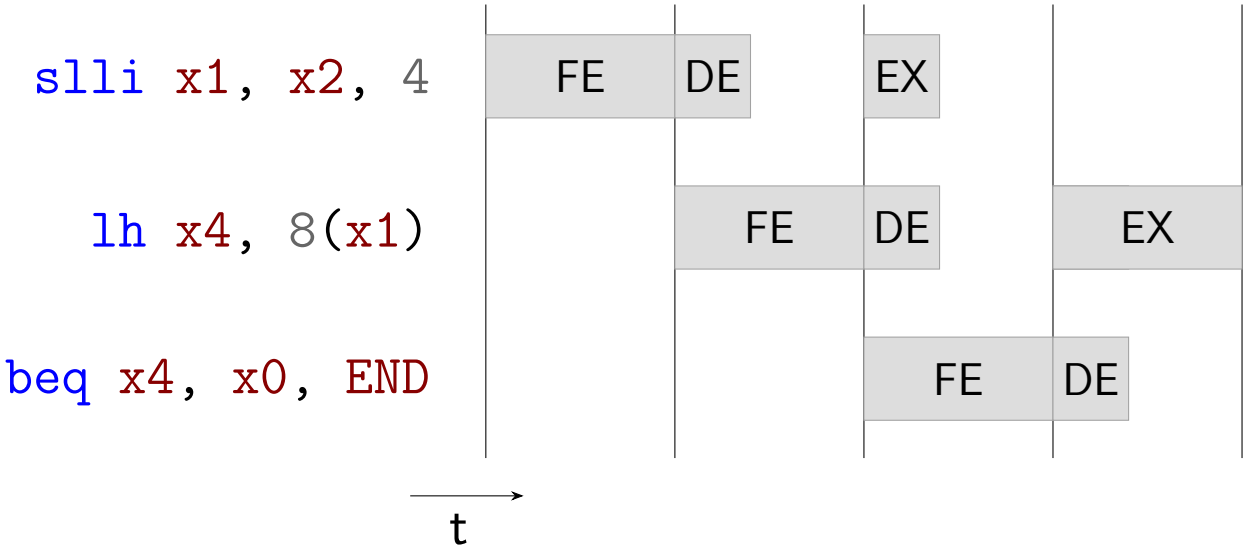

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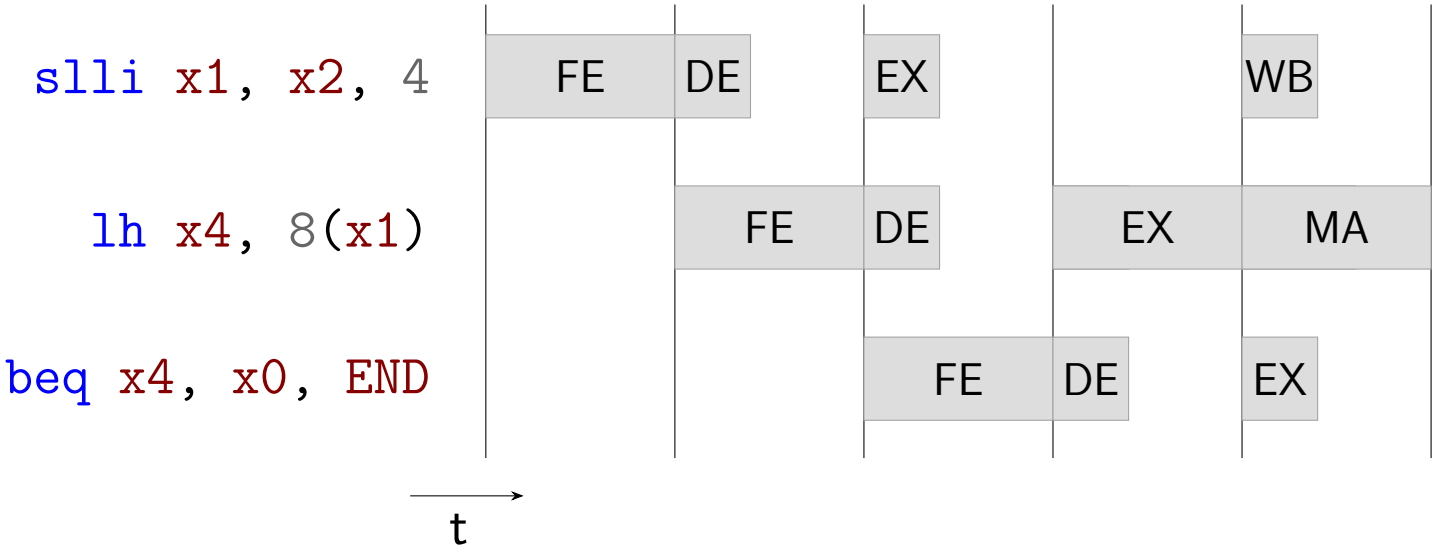

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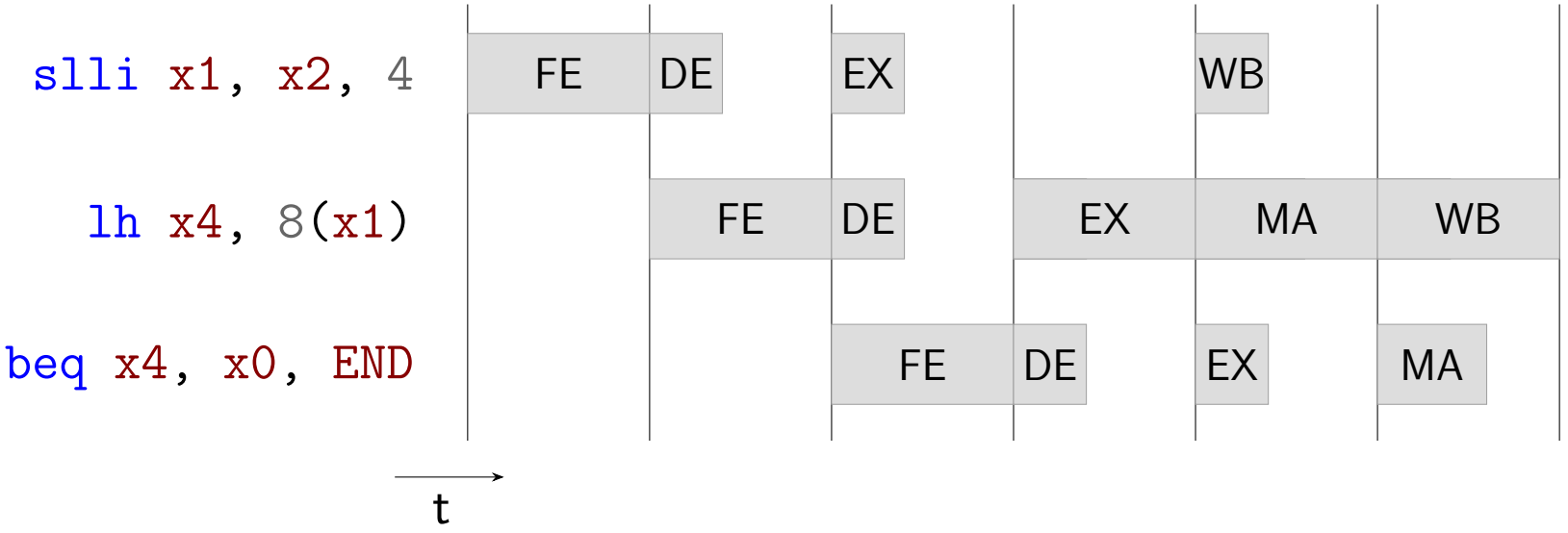

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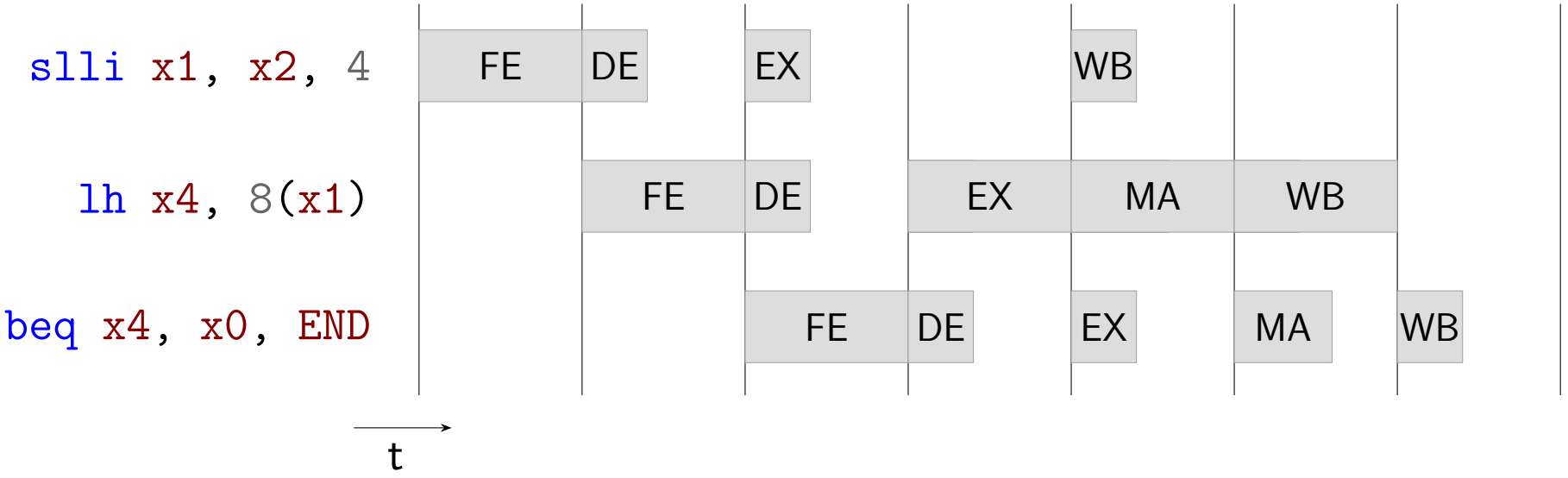

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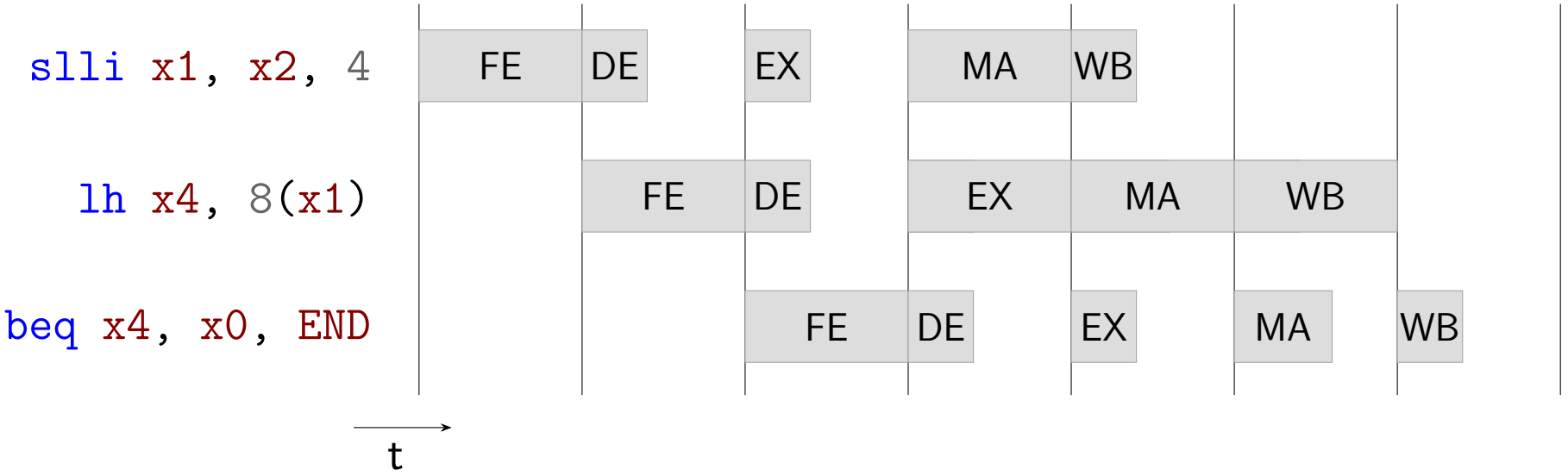

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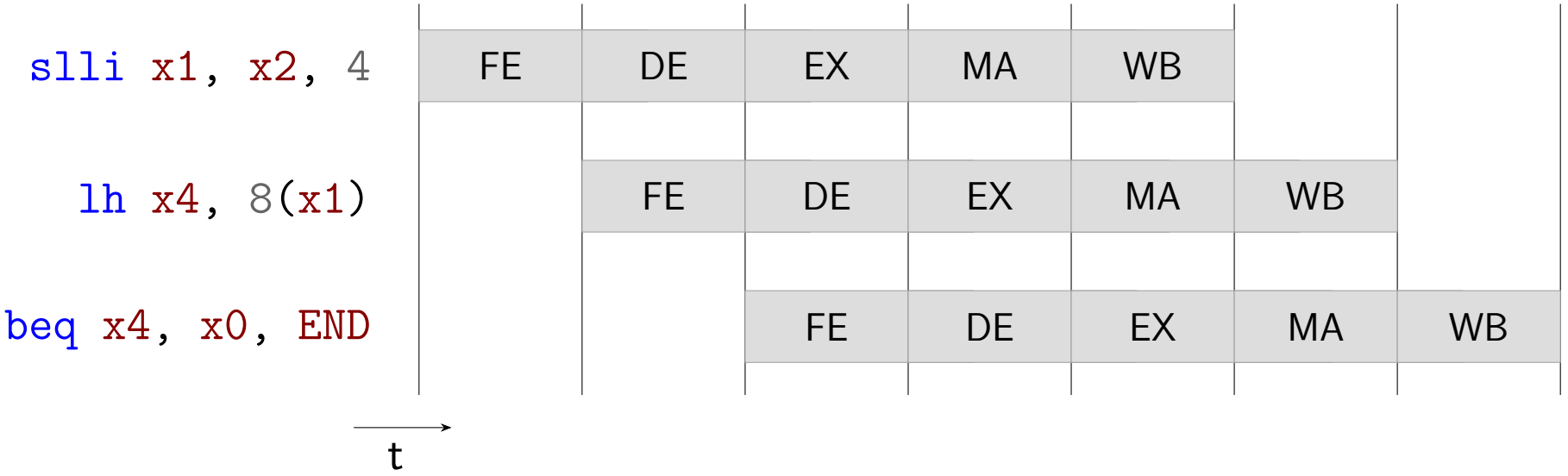

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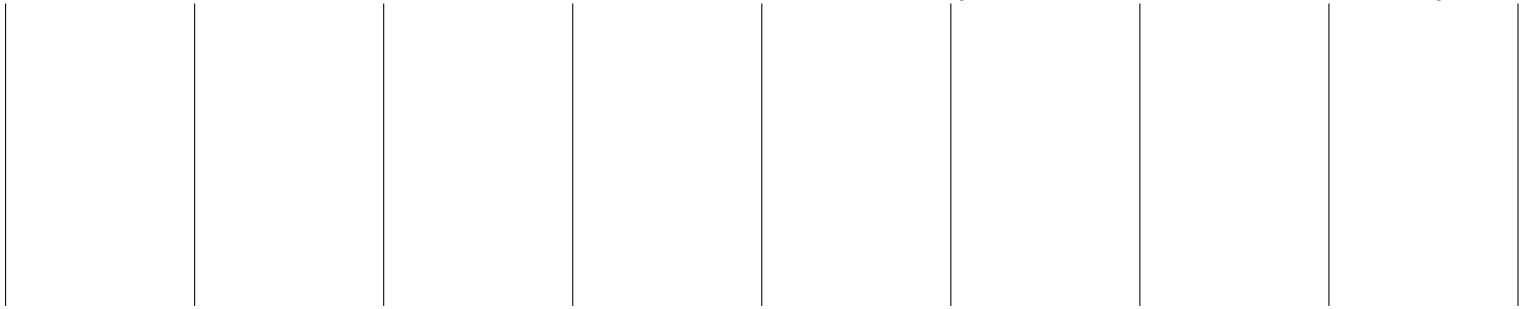
```
   lh x4, 8(x1)

addi x2, x2, 4
```



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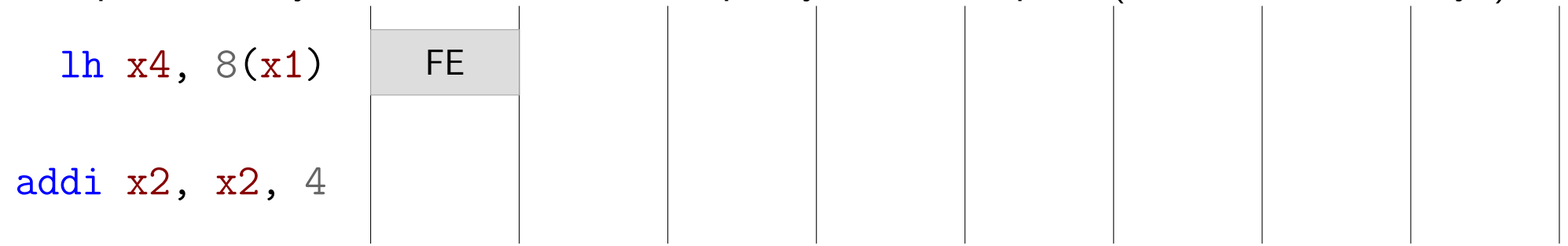

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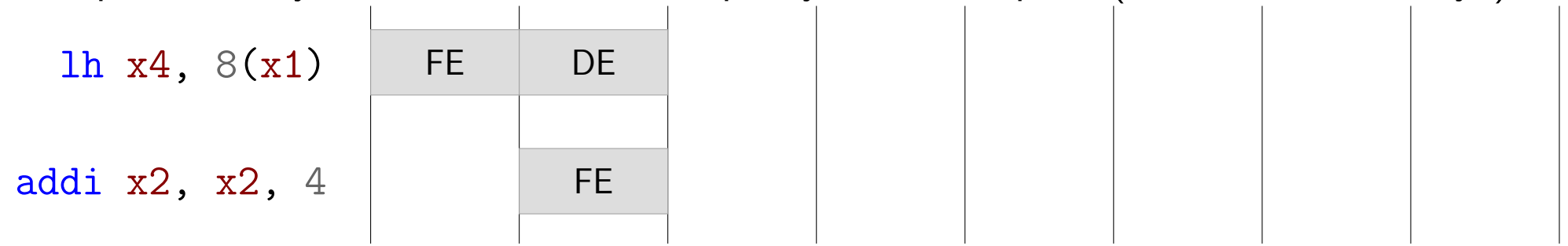

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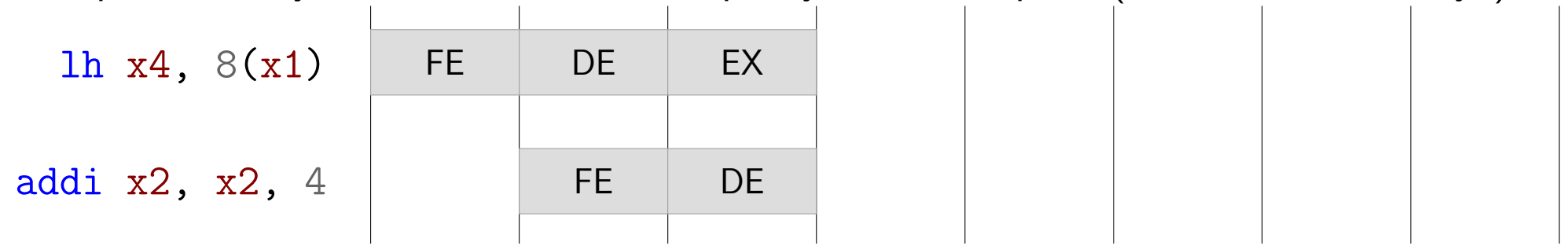

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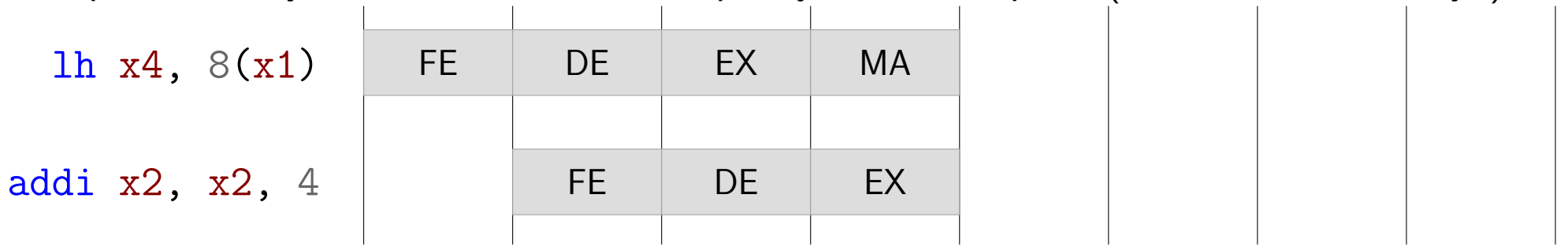

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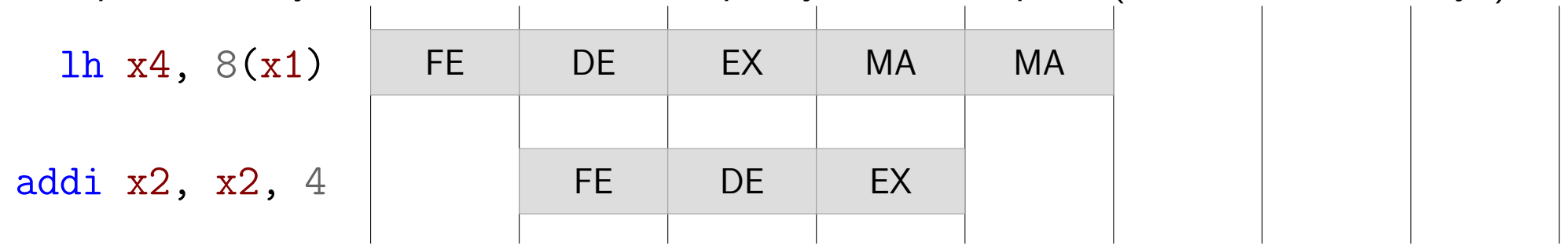

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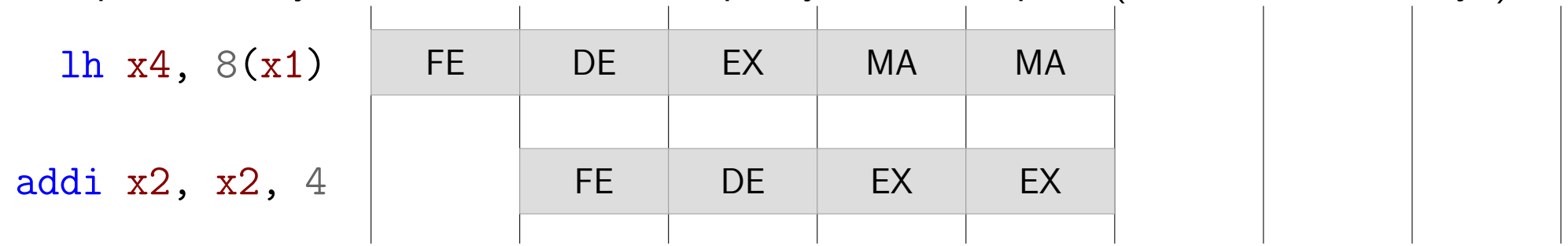

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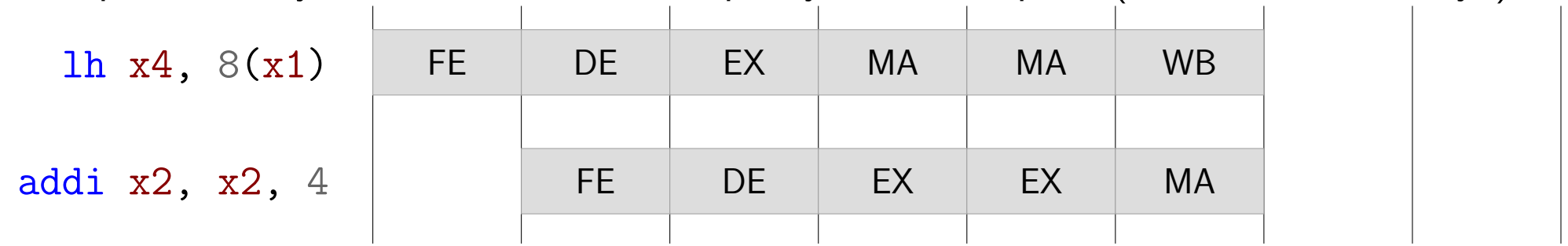

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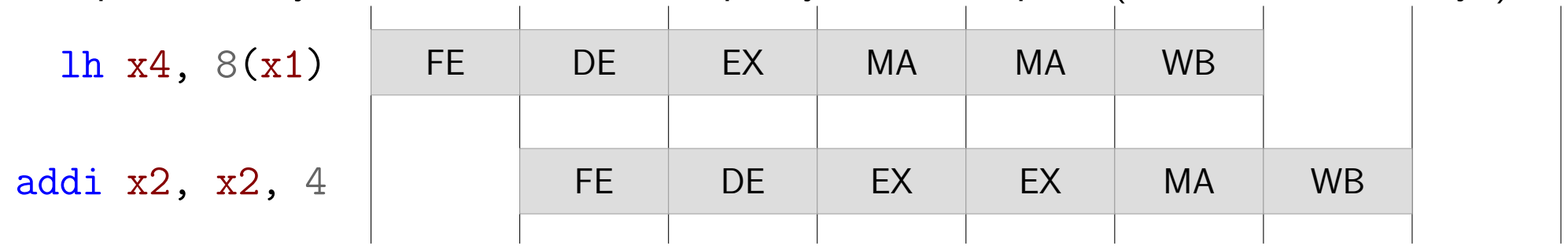

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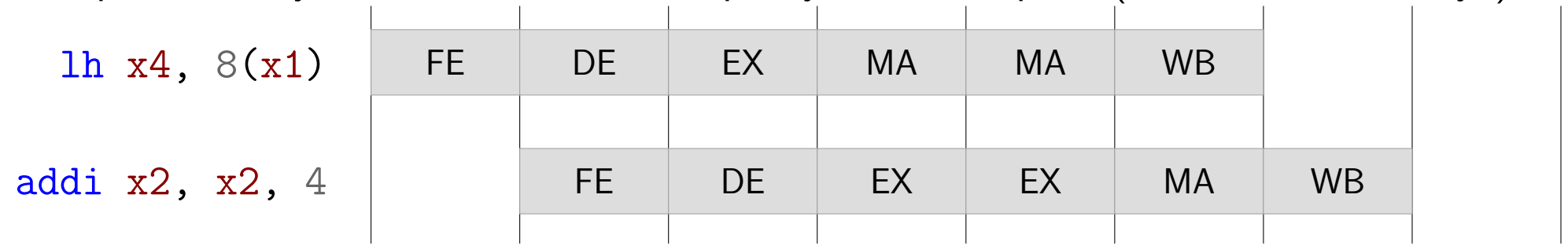

Structural hazards can generally not be avoided!

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Hazards lead to a *pipeline stall* ➔IPC decreases

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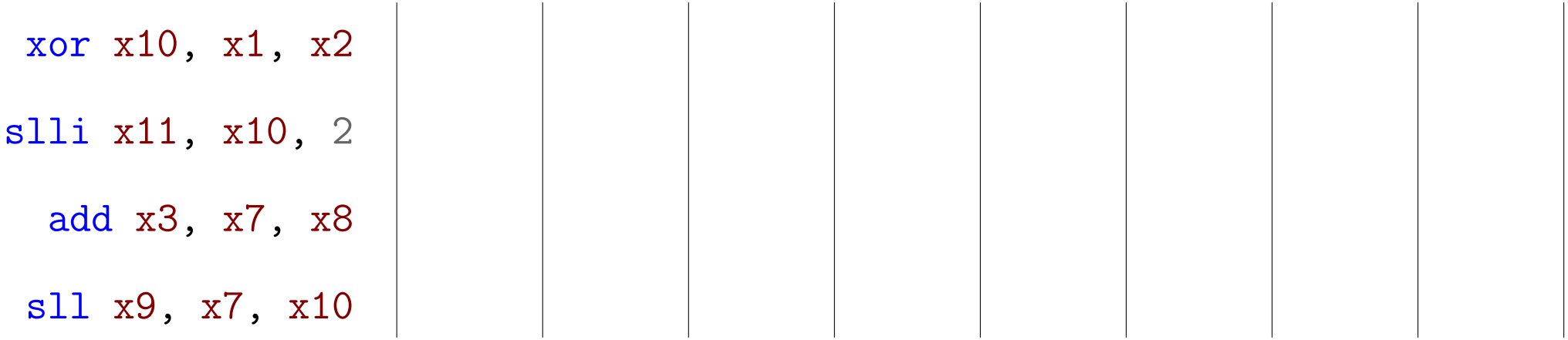

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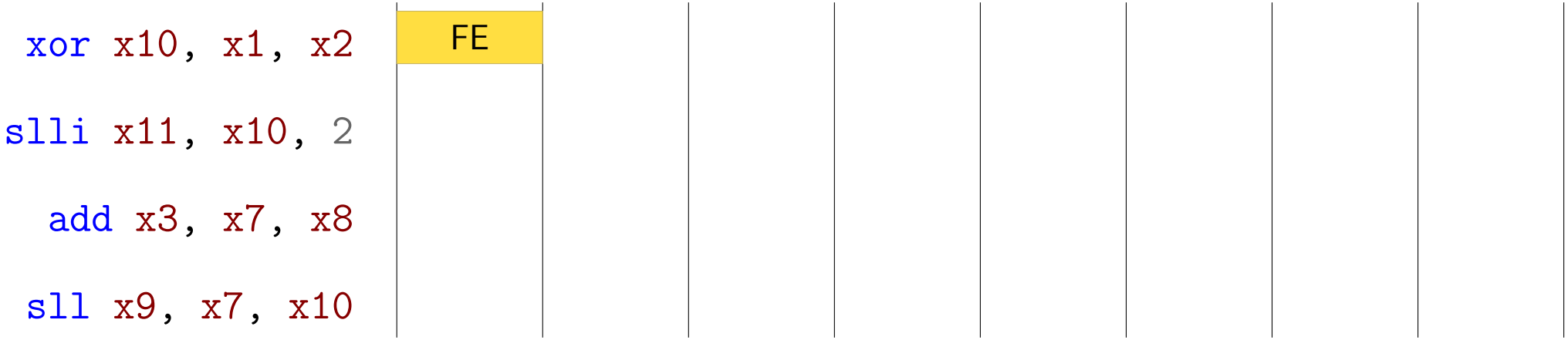

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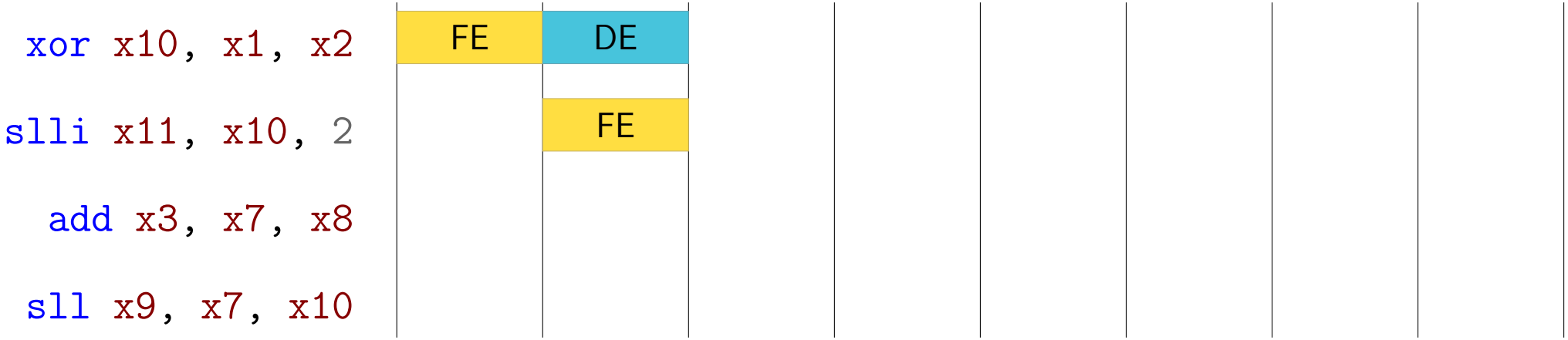

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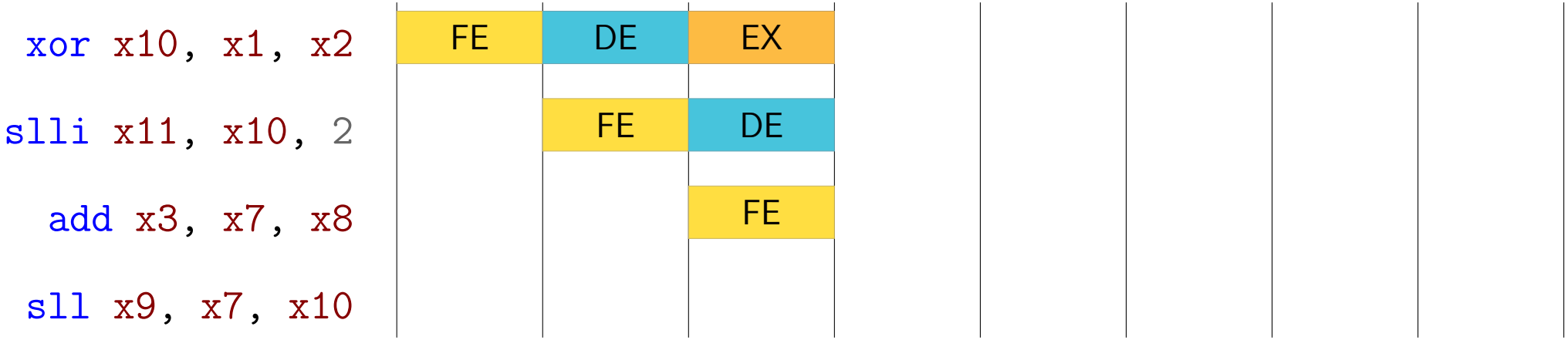

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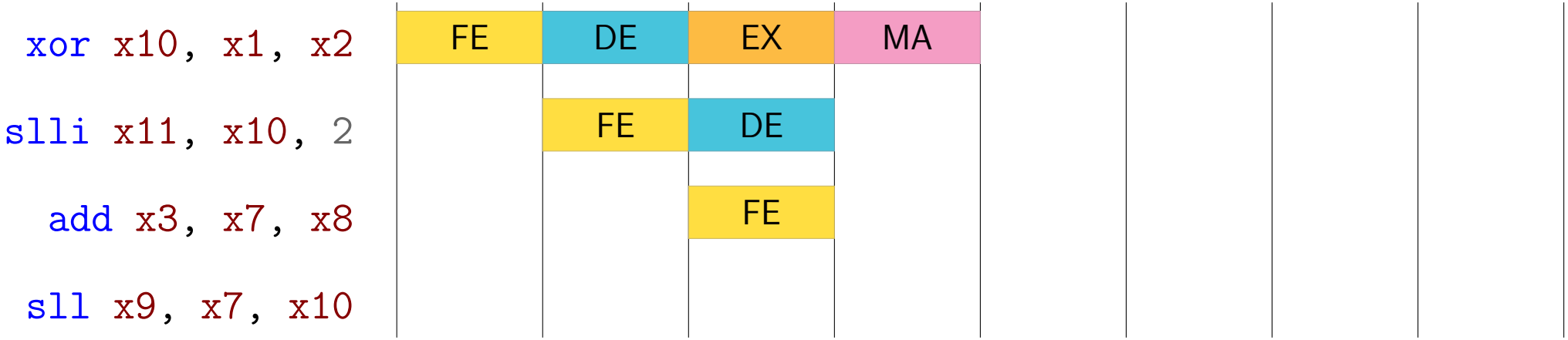

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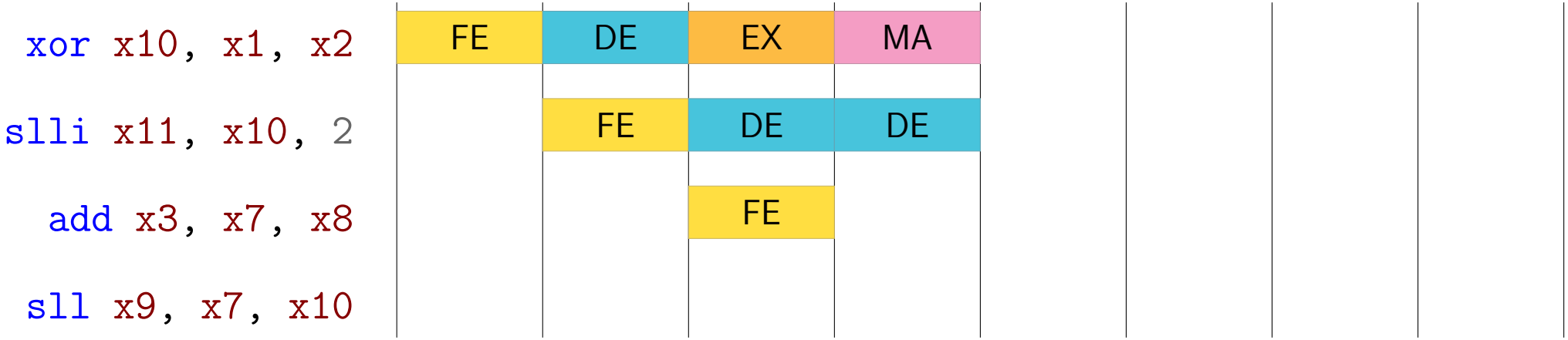

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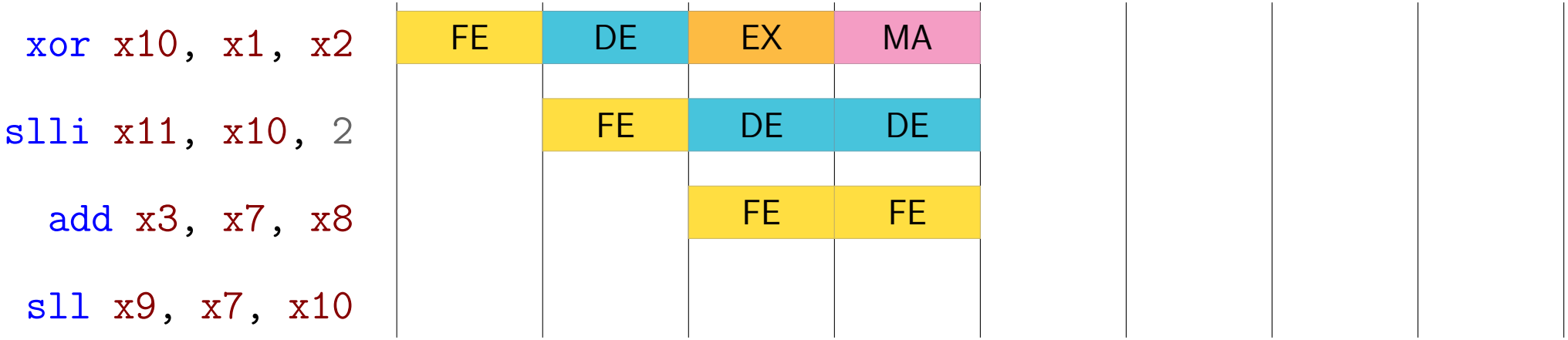

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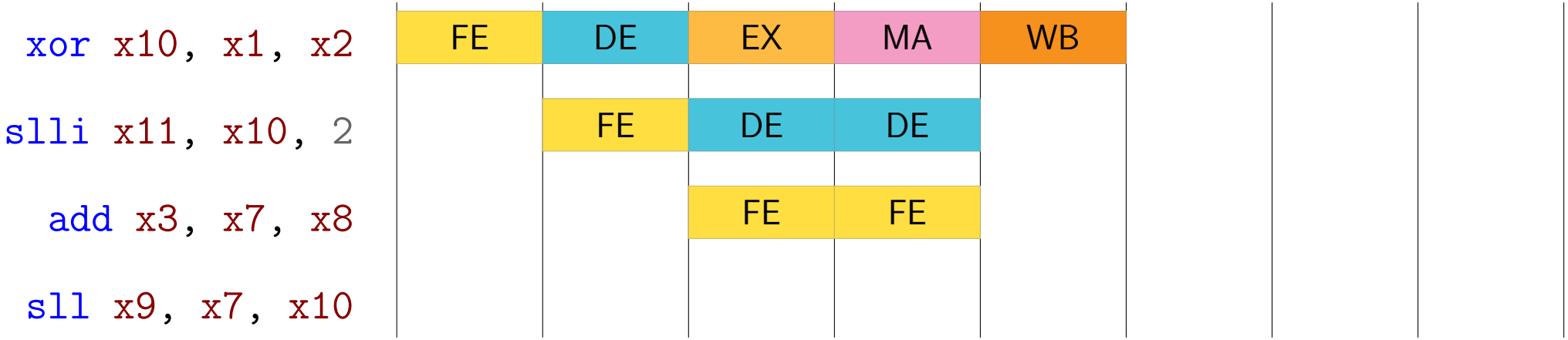

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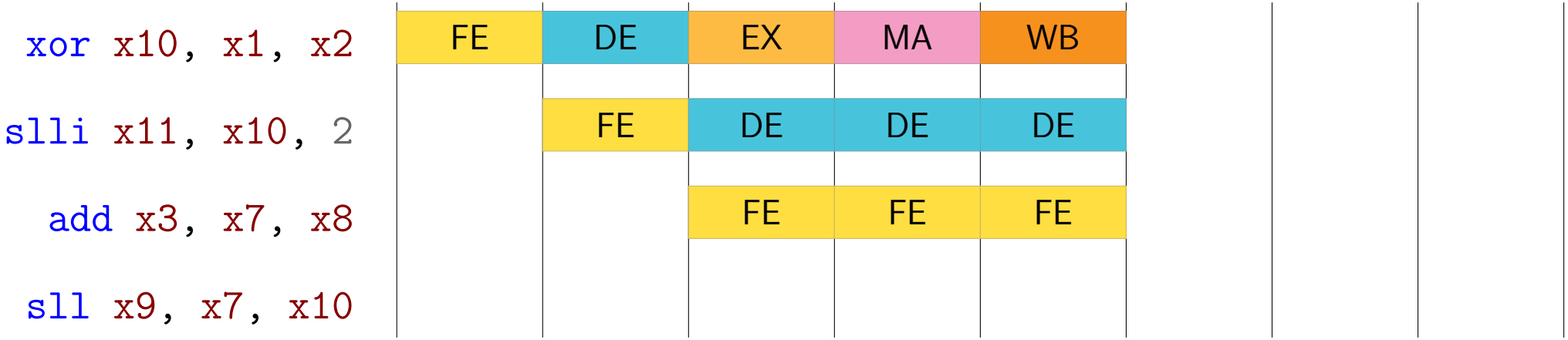

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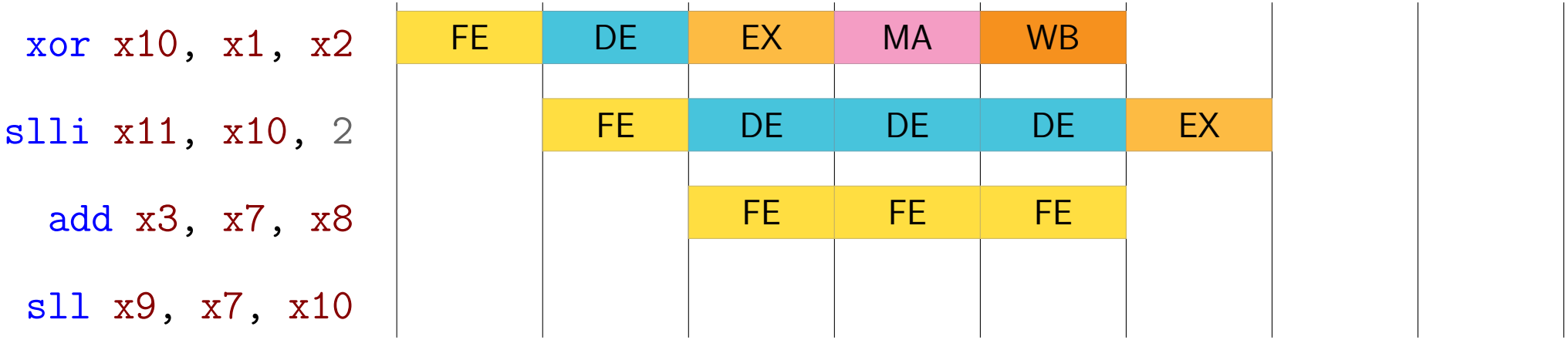

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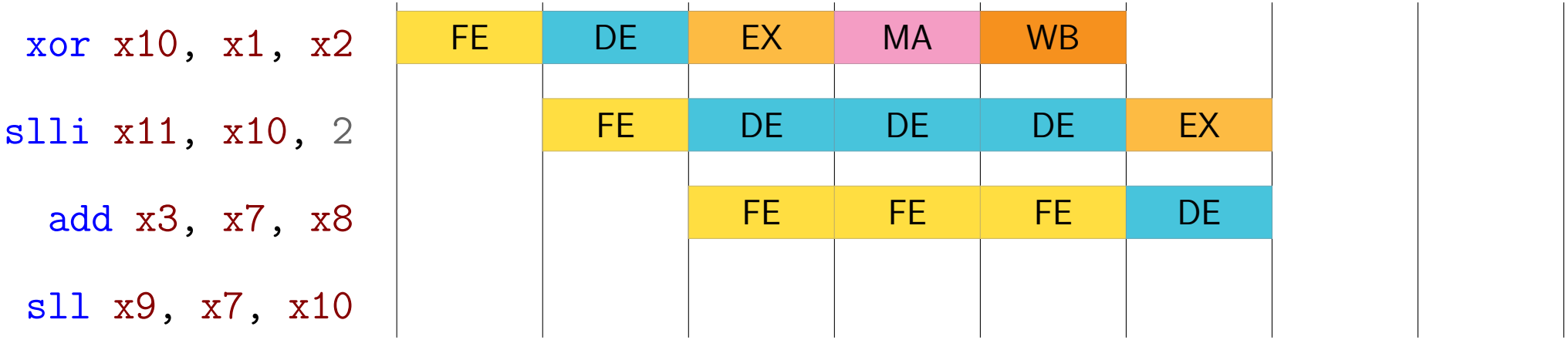

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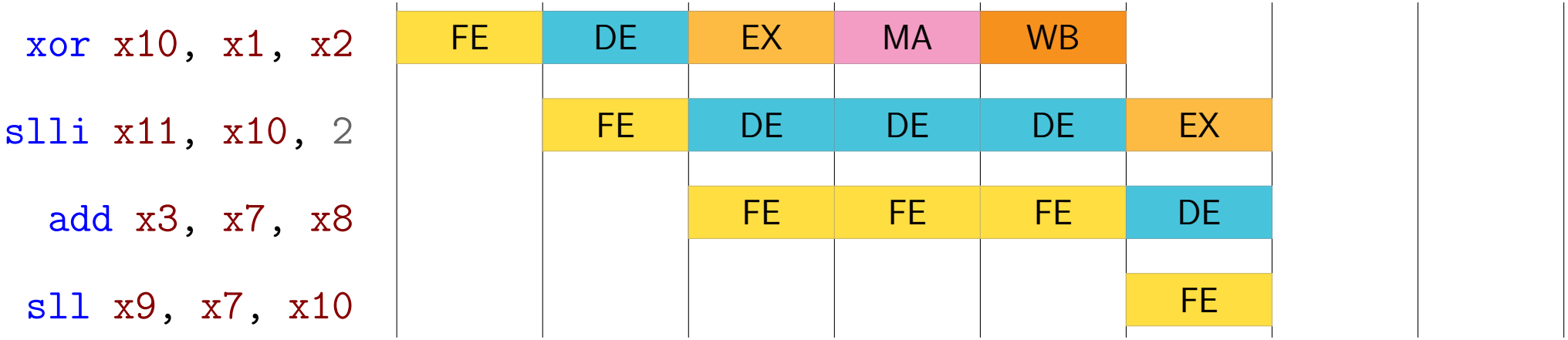

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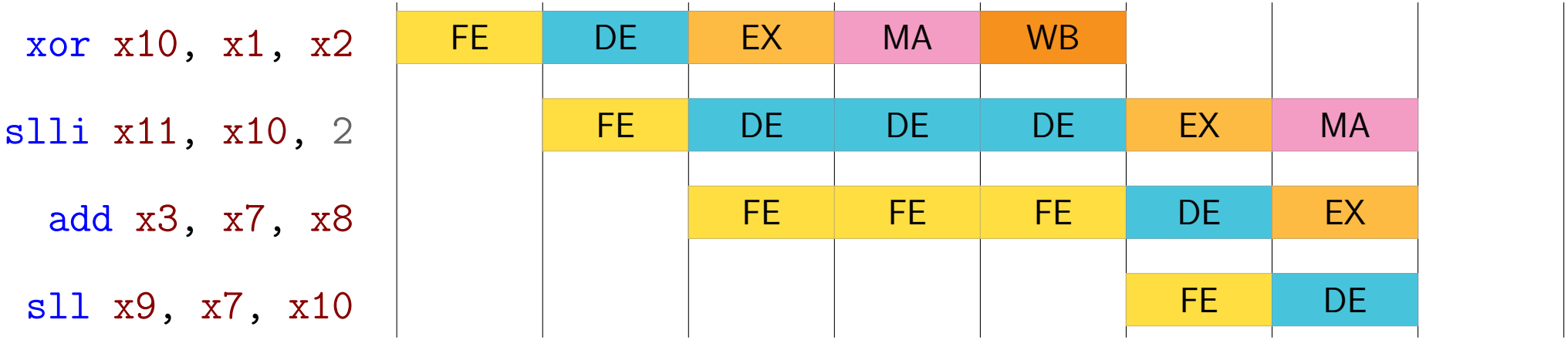

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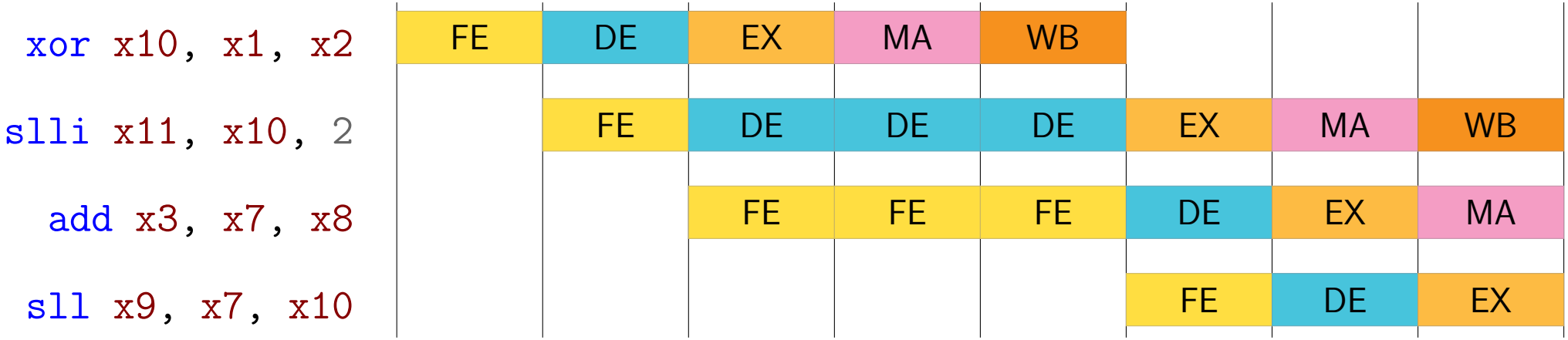

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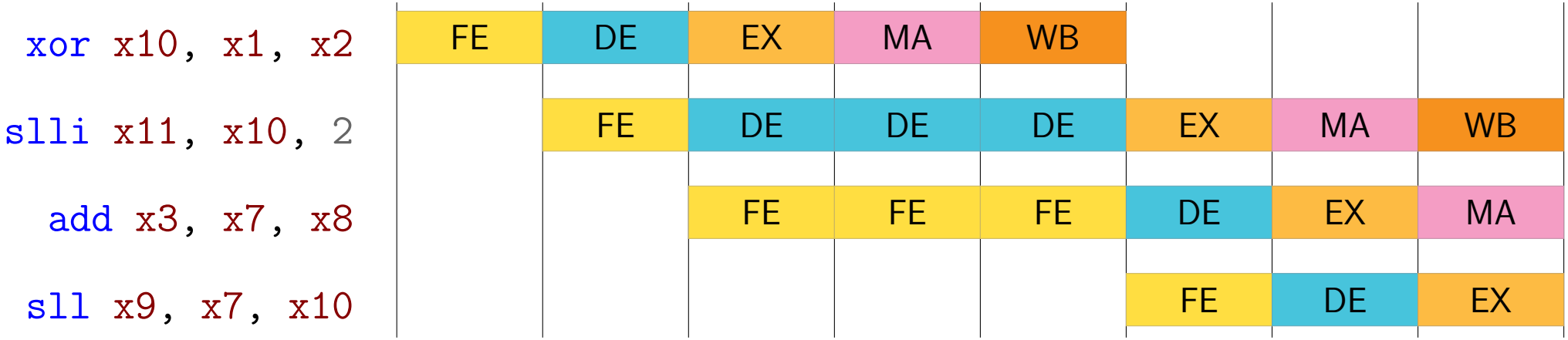

How can we avoid the problem?

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Instruction stream is sequentially stored in memory

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add x3, x7, x8

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Why not execute in any order?

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- Can we reorder instructions?
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Foundation of a large number of optimizations in computer architecture

```
0  xor x10, x1, x2
1  slli x11, x10, 2
2  add x3, x7, x8
3  sll x9, x7, x10
```

Why not execute in any order?

Instruction Level Parallelism

Instruction stream is sequentially stored in memory

But:

- Can we reorder instructions?
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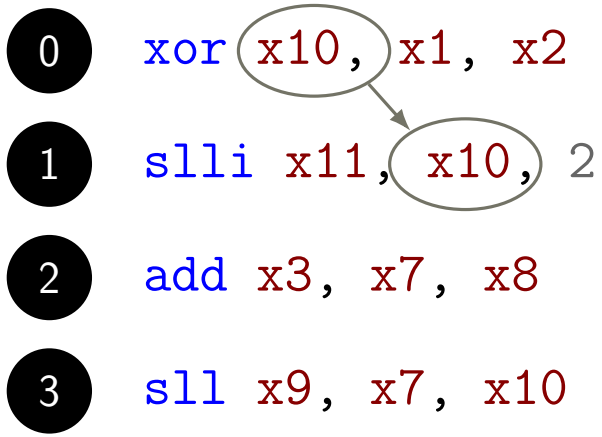

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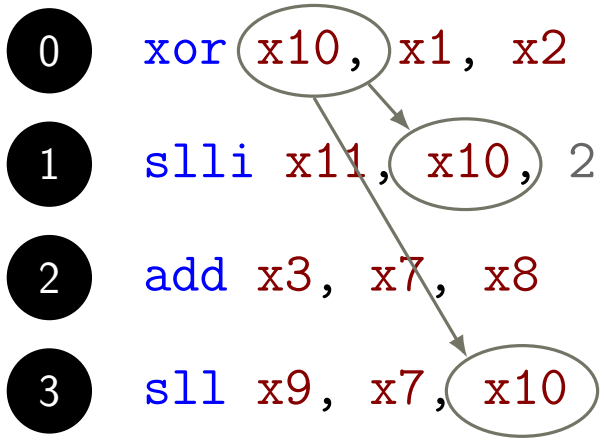

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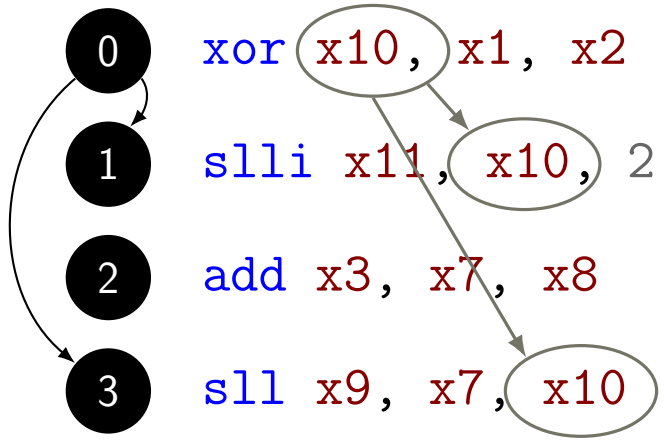

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Reorder instructions

Reorder instructions

Reorder instruction so that the data hazard is resolved

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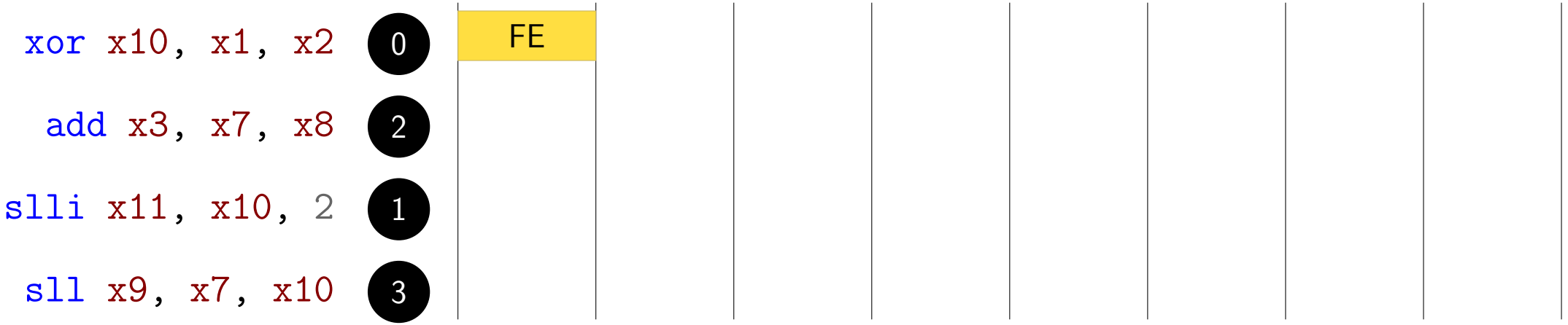

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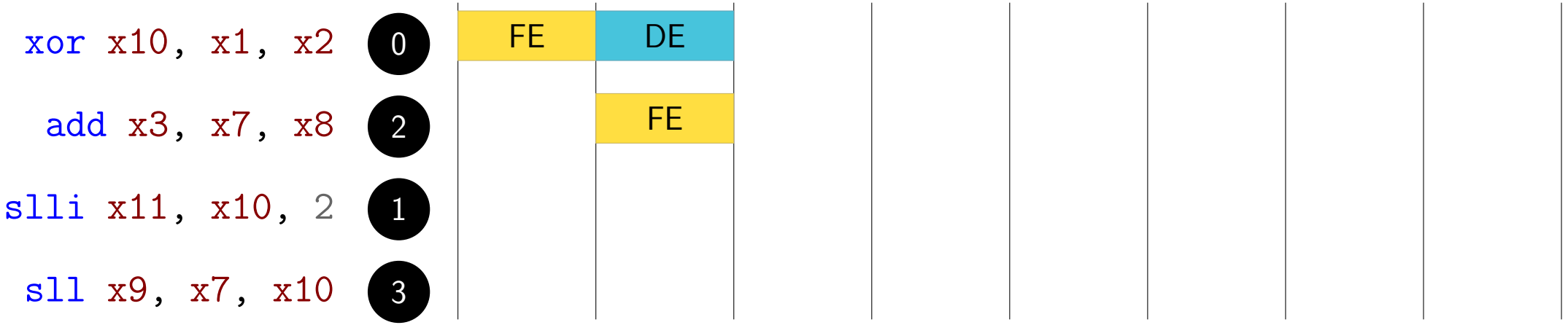

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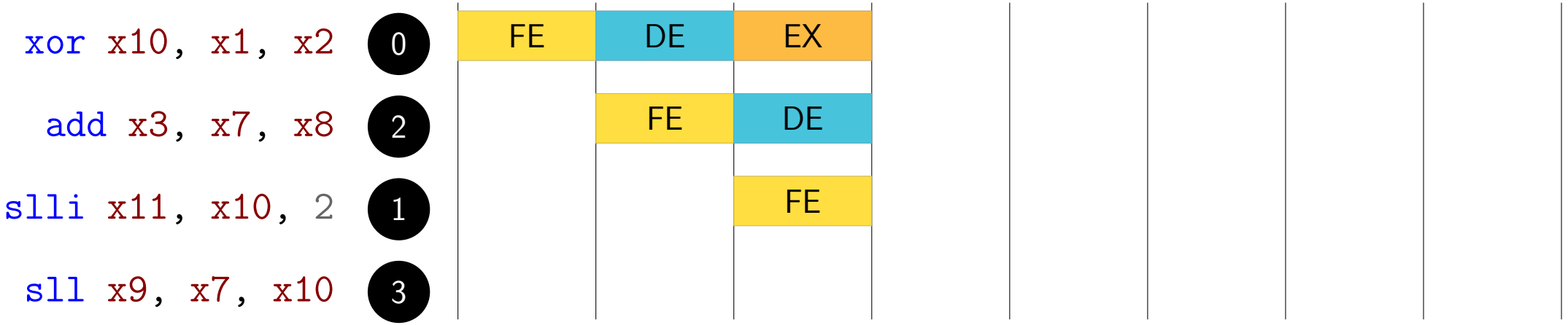

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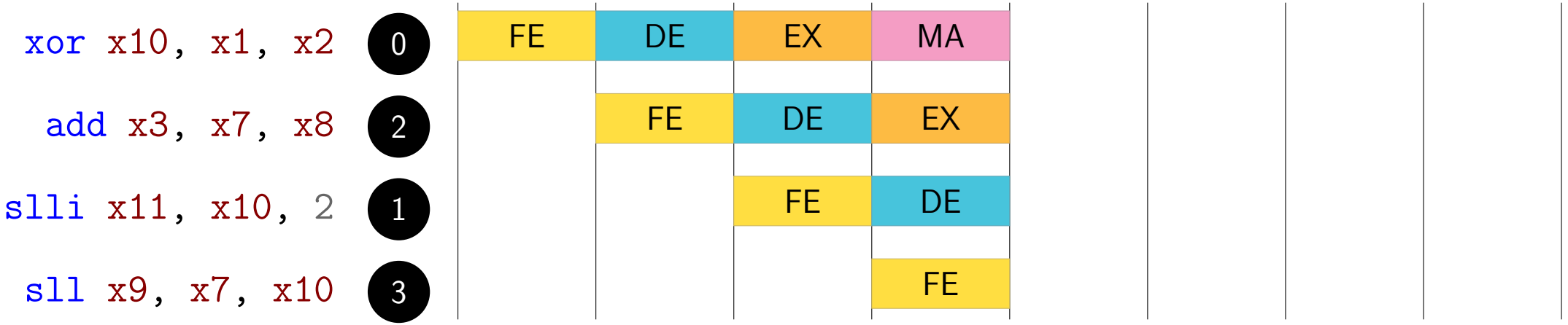

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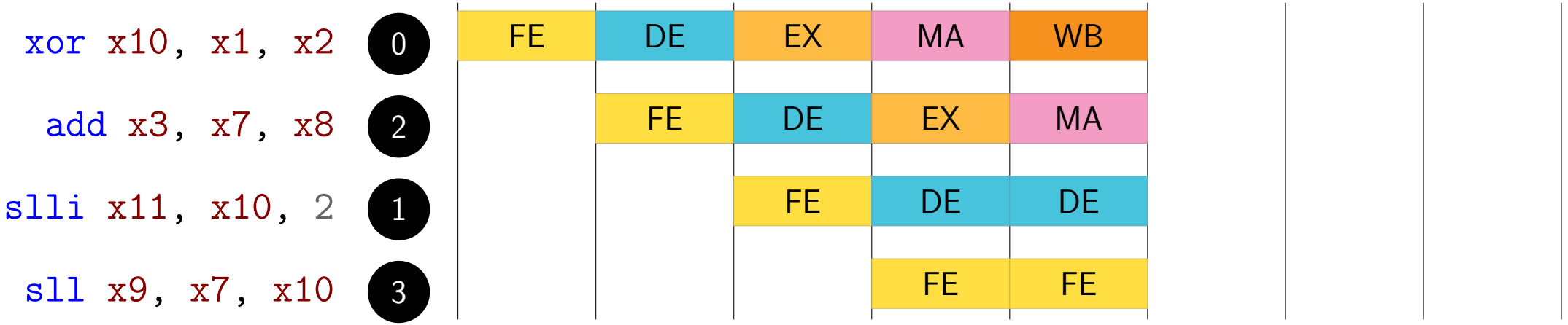

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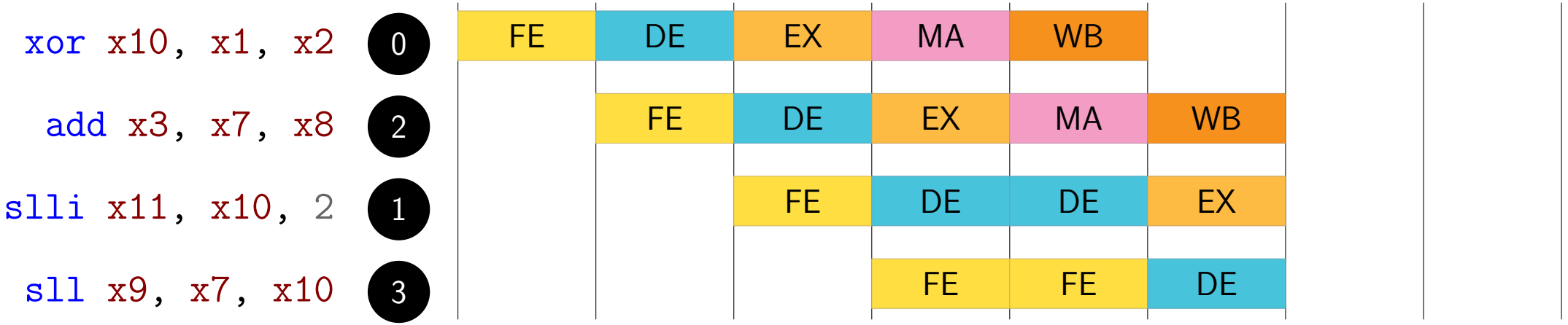

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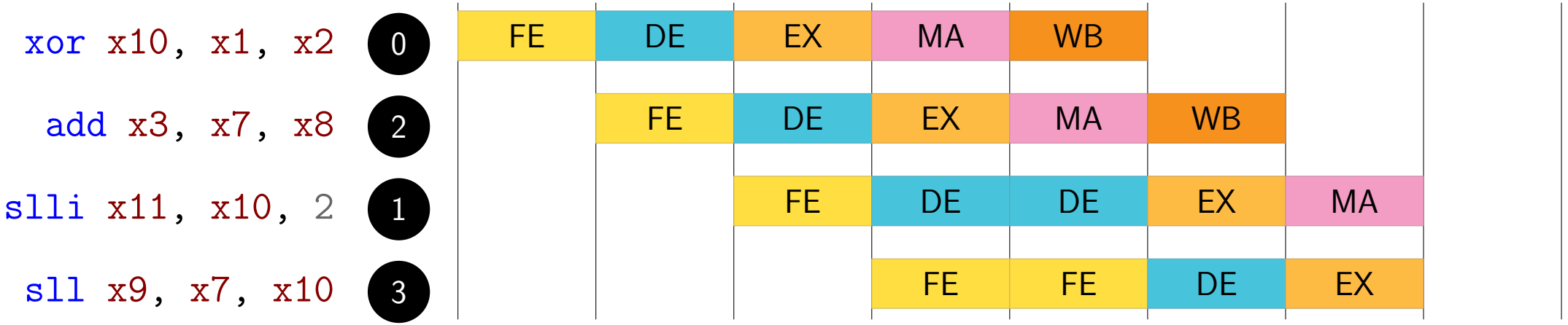

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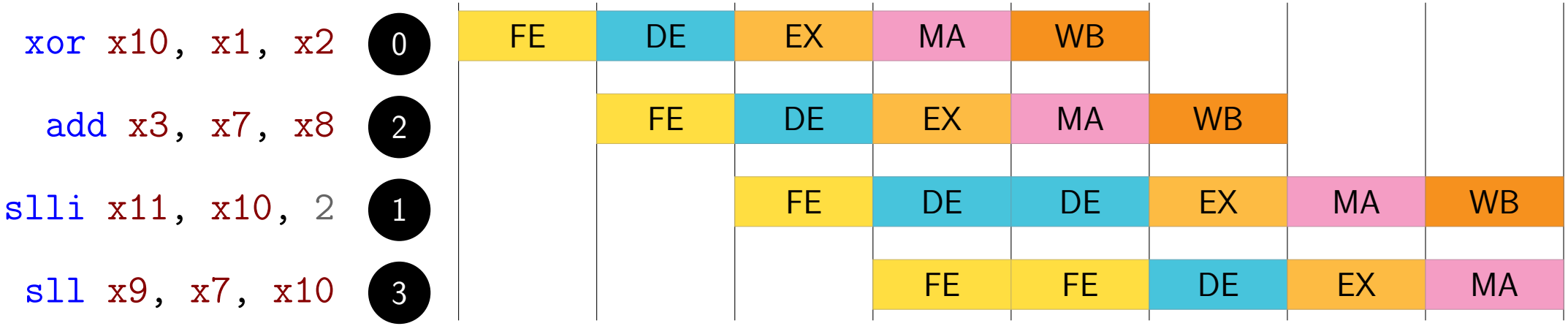

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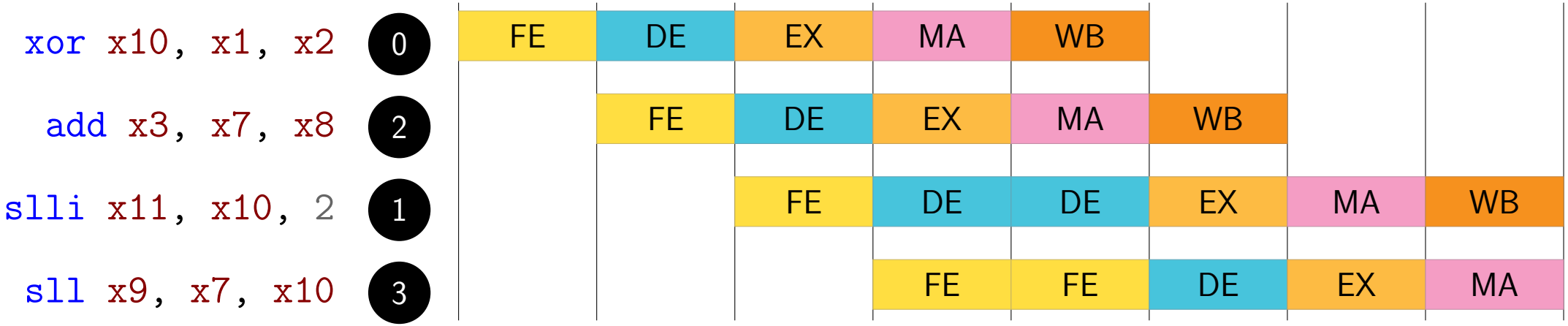

Reordering limited, especially with "deeper" (more stages) pipelines

Pipeline Forwarding

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Reordering instructions has limitations

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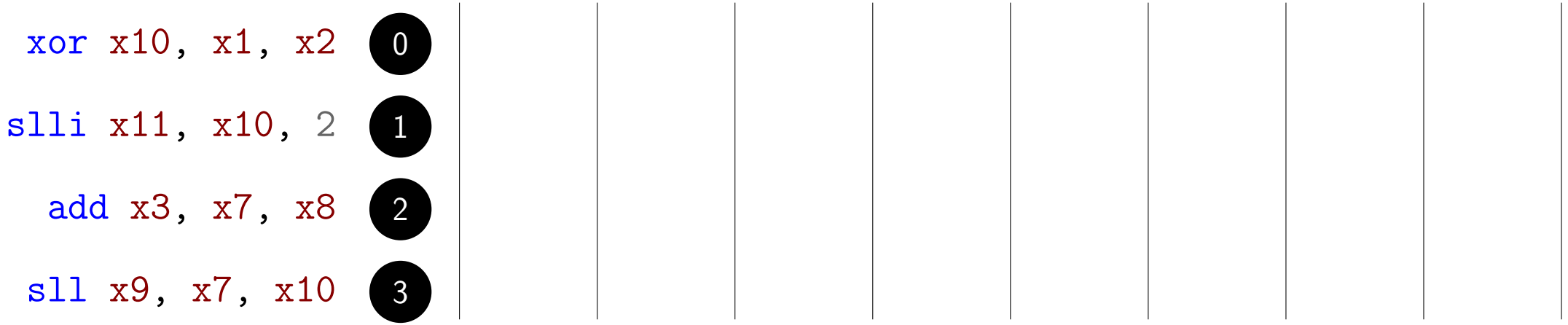
Pipeline Forwarding: Make result available to earlier stages before writeback



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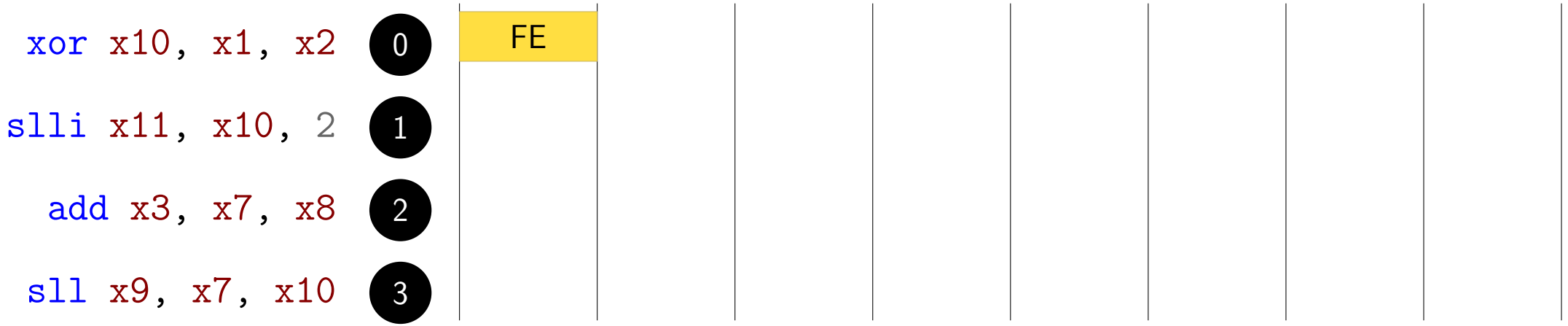

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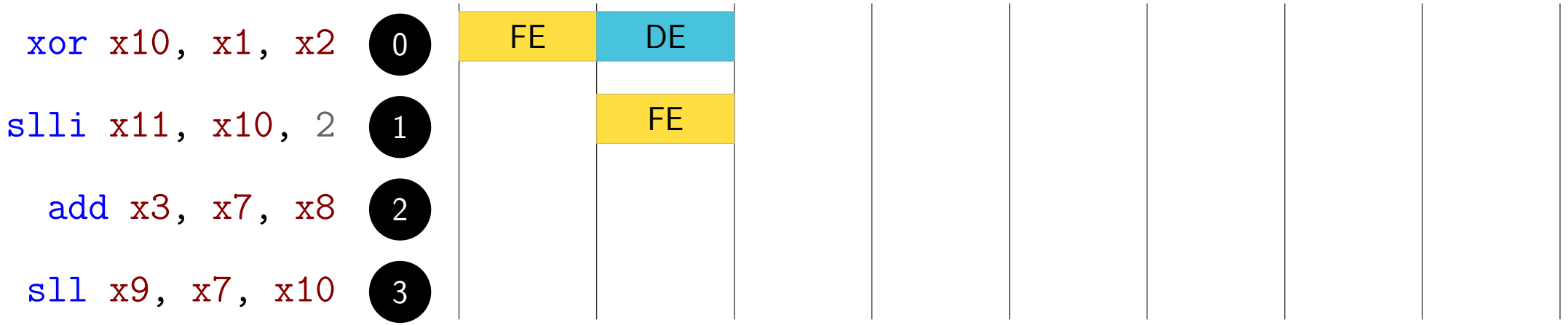

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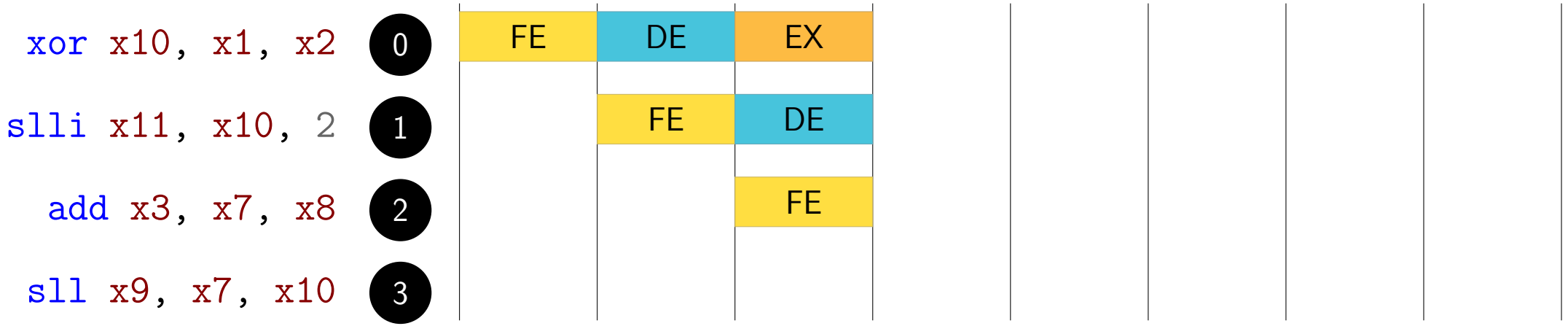

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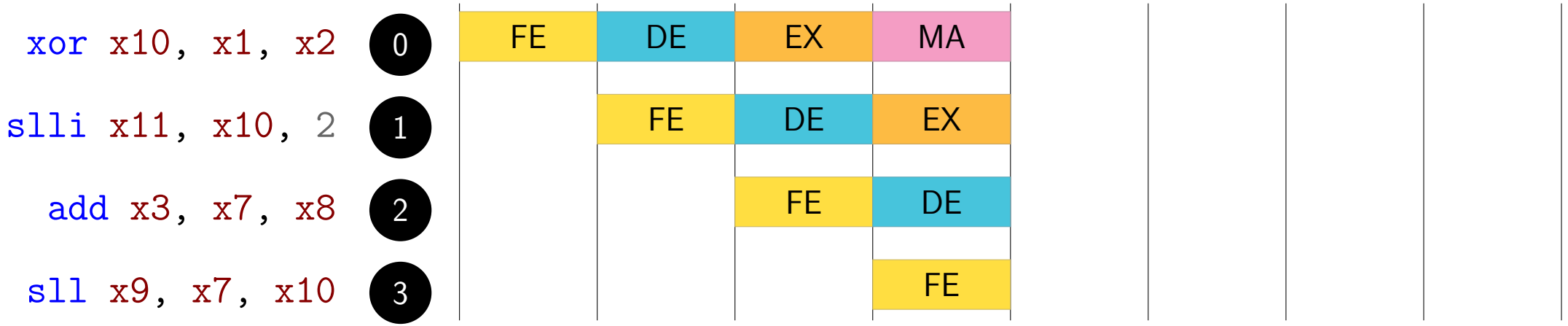

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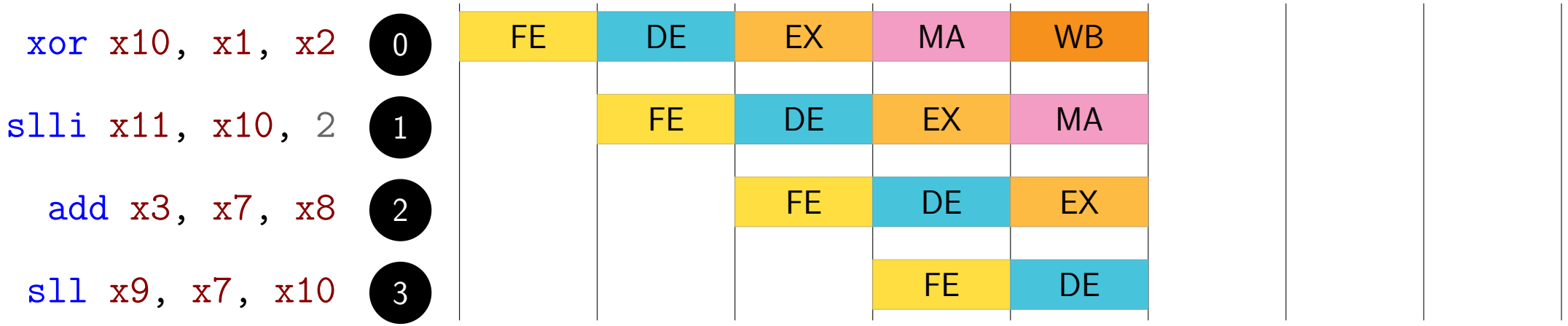

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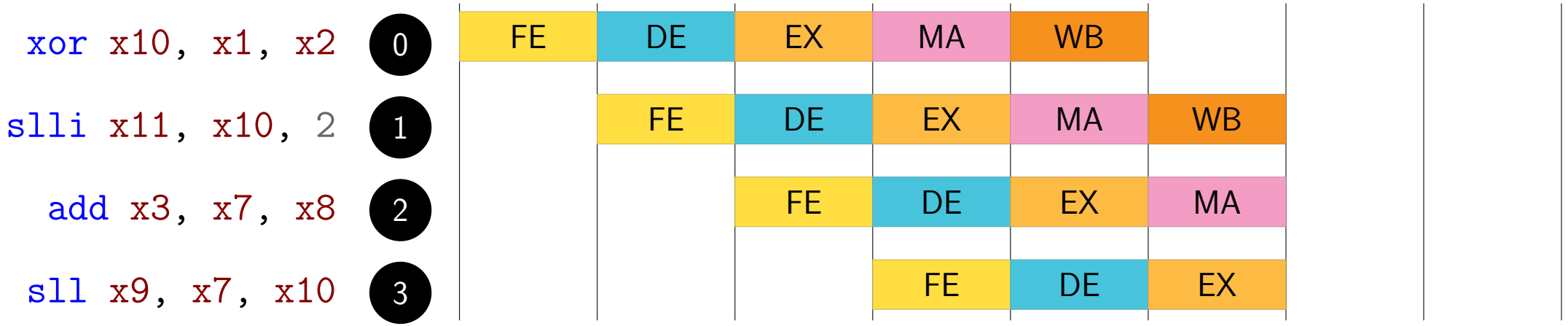

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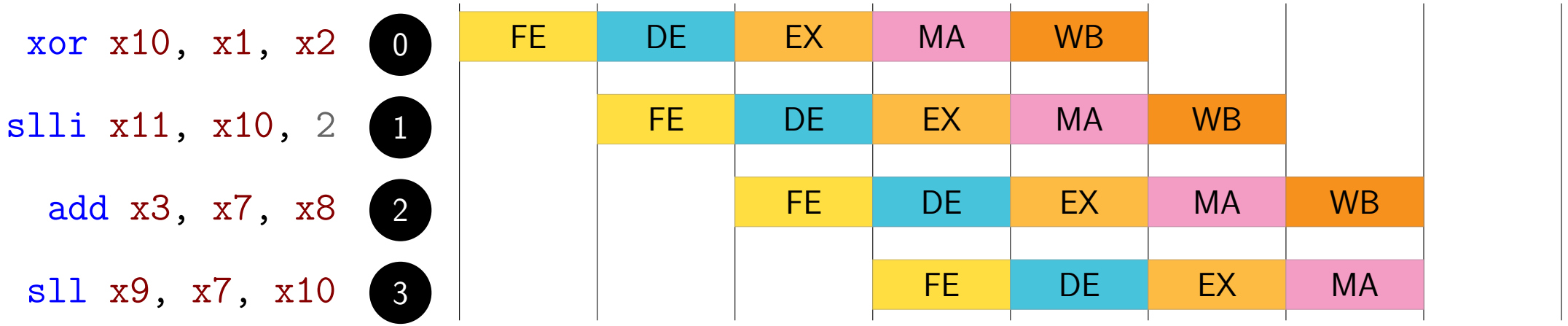

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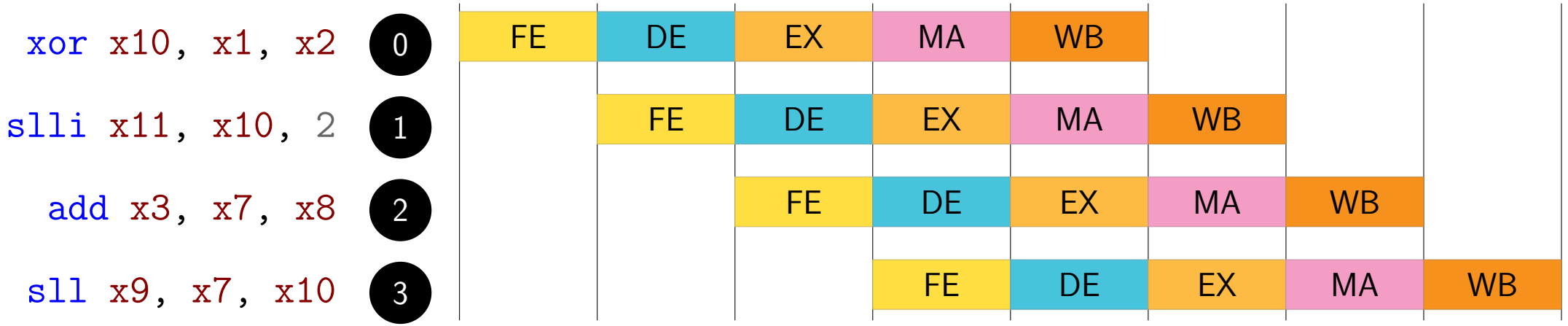
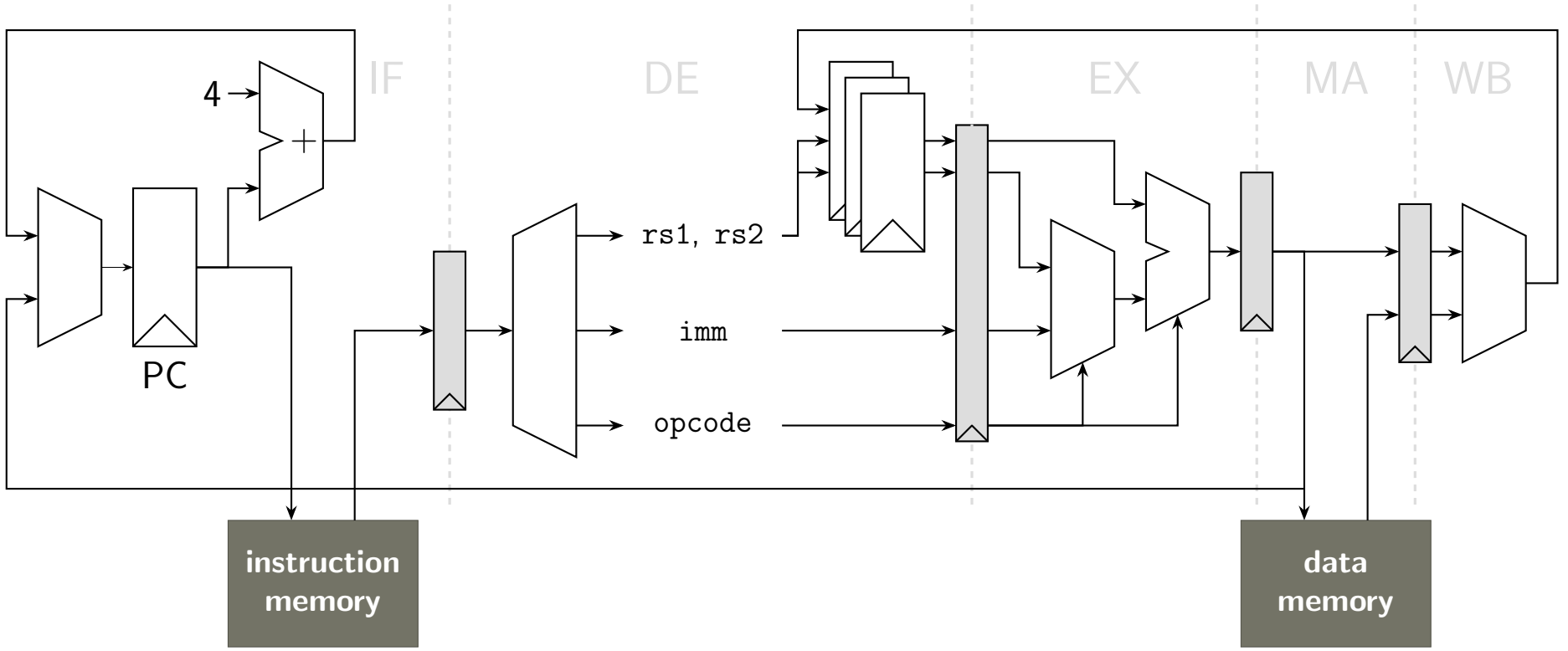


Pipeline Forwarding (simplified)



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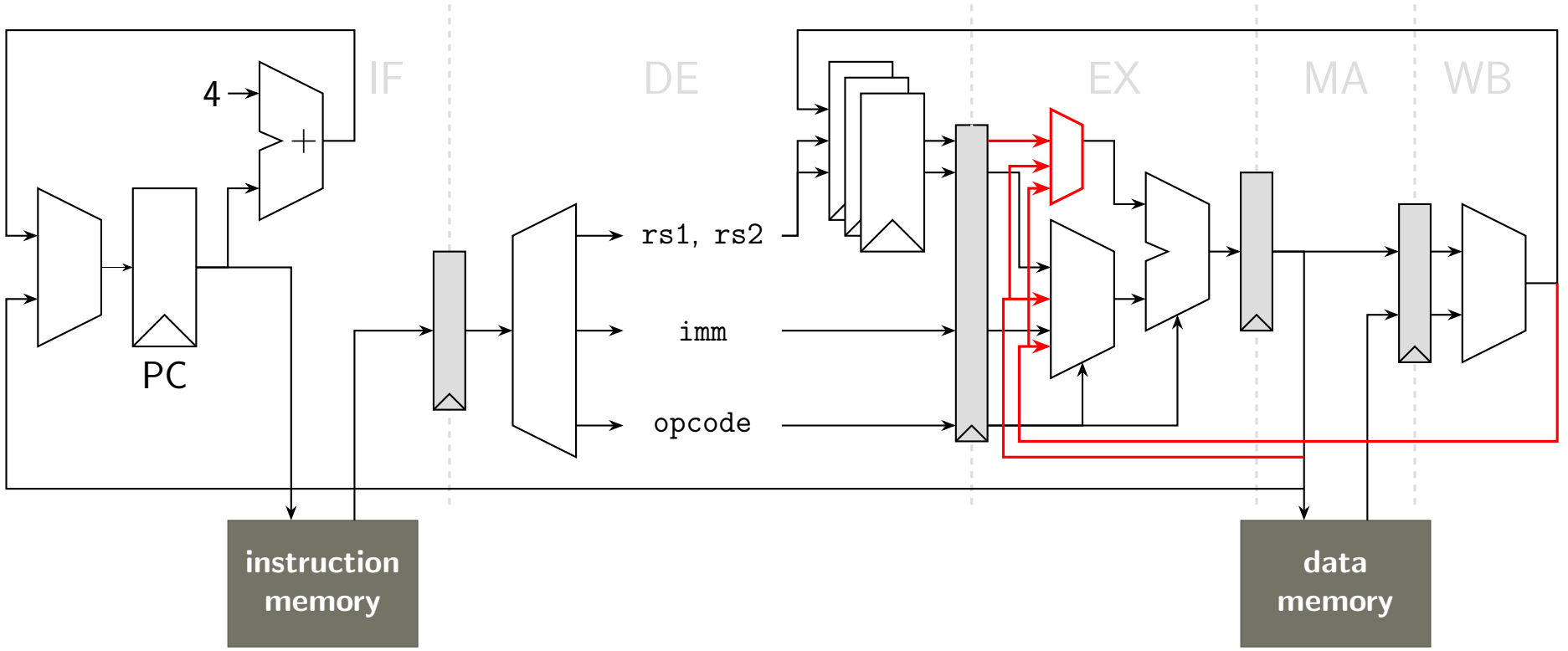

Data Hazard (continued)

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Are we fine now?

```
  lw x4, 8(x2)
addi x5, x4, 3
sll x6, x4, x5
andi x5, x6, 3
  sw x5, 4(x2)
```


Data Hazard (continued)

Are we fine now?

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  lw x4, 8(x2)
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There are other data dependencies

Background: Variables and Registers

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Compiler generates intermediate representation: instructions from code, variables as symbols

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Example: Static Single Assignment Form (*versions* of variables)

```
int f(int *a, int b) {
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}
```

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}
```

```
define i32 @f(i32* %0, i32 %1) #0 {
  %3 = load i32, i32* %0, align 4
  %4 = getelementptr inbounds i32, i32* %0, i64 1
  %5 = load i32, i32* %4, align 4
  %6 = getelementptr inbounds i32, i32* %0, i64 2
  %7 = load i32, i32* %6, align 4
  %8 = sub i32 %3, %1
  %9 = add i32 %8, %5
  %10 = add i32 %9, %7
  ret i32 %10
}
```

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```

At this point we only have the data dependencies from above

Background: Register Allocation


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```

```
f:
  lw   a2, 0(a0)

  lw   a3, 4(a0)

  lw   a0, 8(a0)
  sub  a1, a2, a1
  add  a1, a1, a3
  addw a0, a0, a1
  ret
```

Problem: Registers are scarce (RISC-V 31, minus ABI registers)

Background: Register Allocation

Compiler generates machine code, unbound number of symbols must be mapped to registers

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define i32 @f(i32* %0, i32 %1) #0 {
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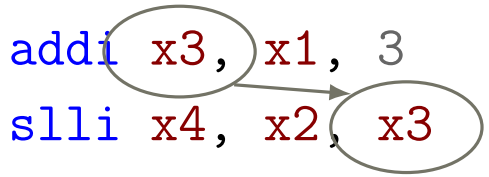

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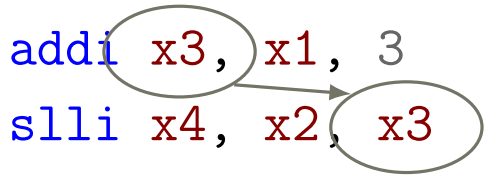

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addi x3, x5, 7
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Read-after-Read is not a hazard

Data Flow Graph

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Data flow graph can be used to identify instruction level parallelism

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Graph of data dependencies

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0 `lw x4, 8(x2)`

1 `addi x5, x4, 3`

2 `sll x6, x4, x5`

3 `andi x5, x6, 3`

4 `sw x5, 4(x2)`

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Data flow graph can be used to identify instruction level parallelism

Graph of data dependencies

- Each instruction is a *vertex*
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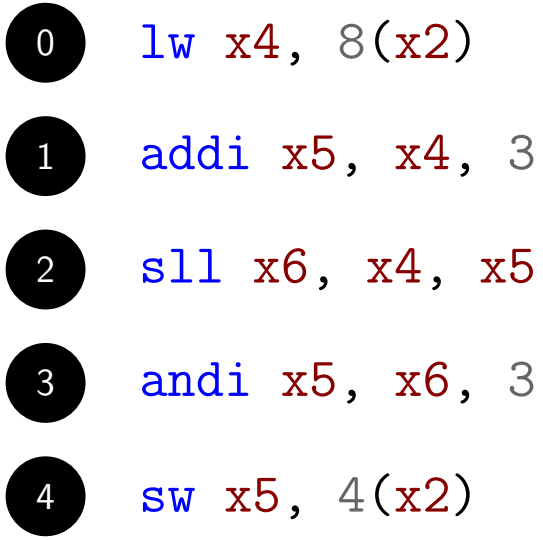

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Graph of data dependencies

- Each instruction is a *vertex*
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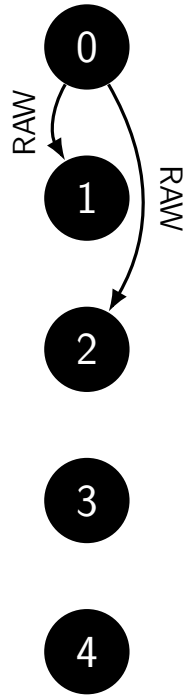

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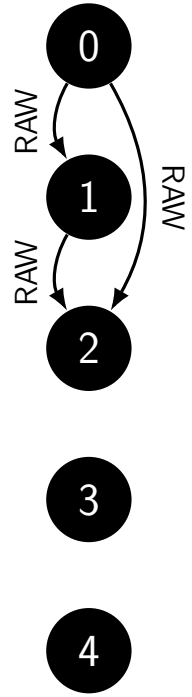

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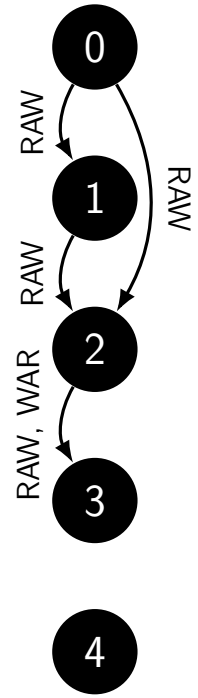

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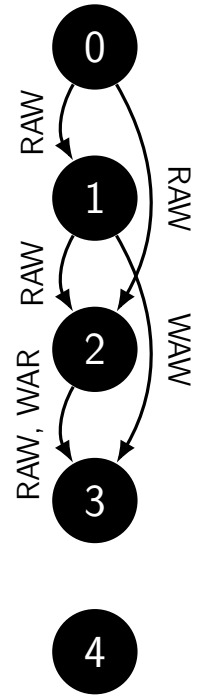

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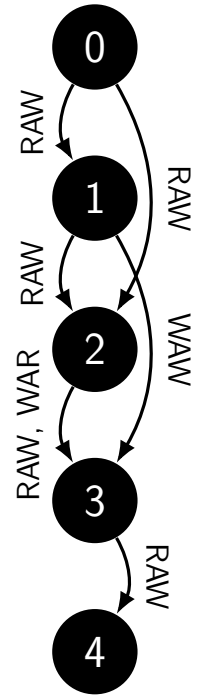

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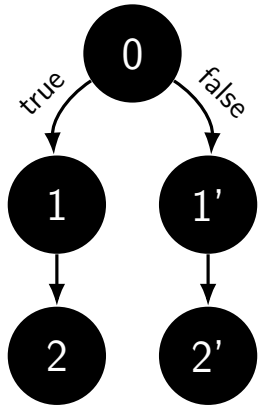

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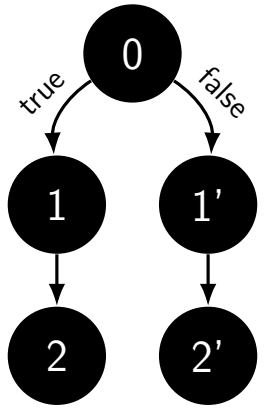

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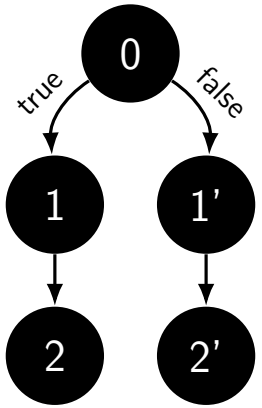

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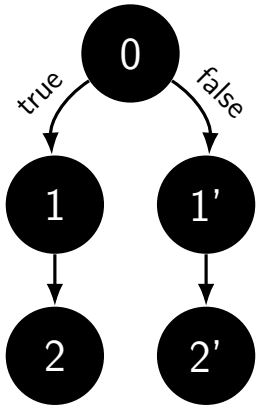


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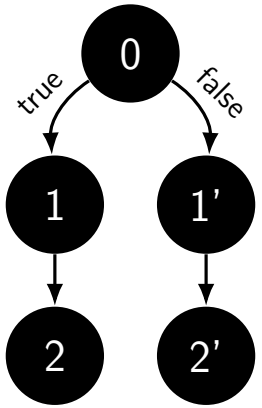

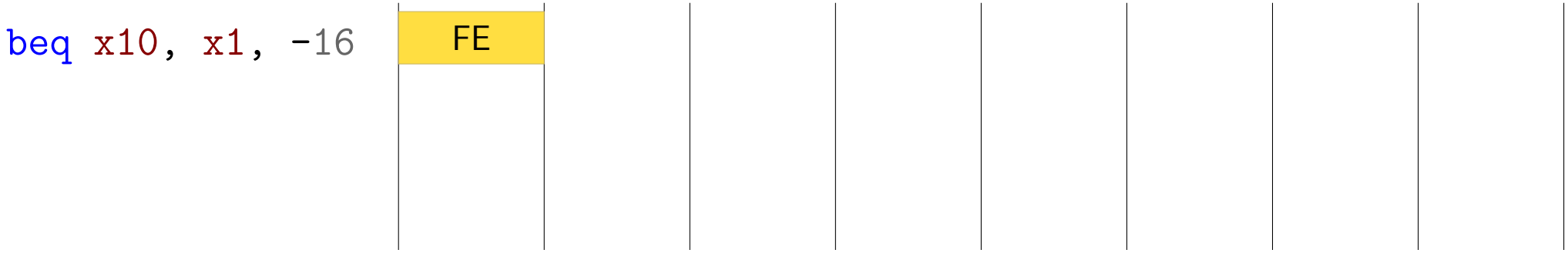

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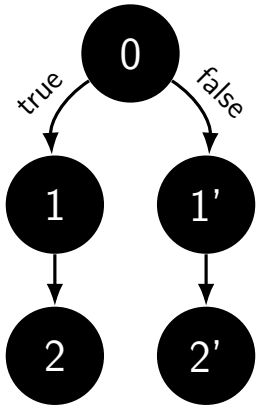


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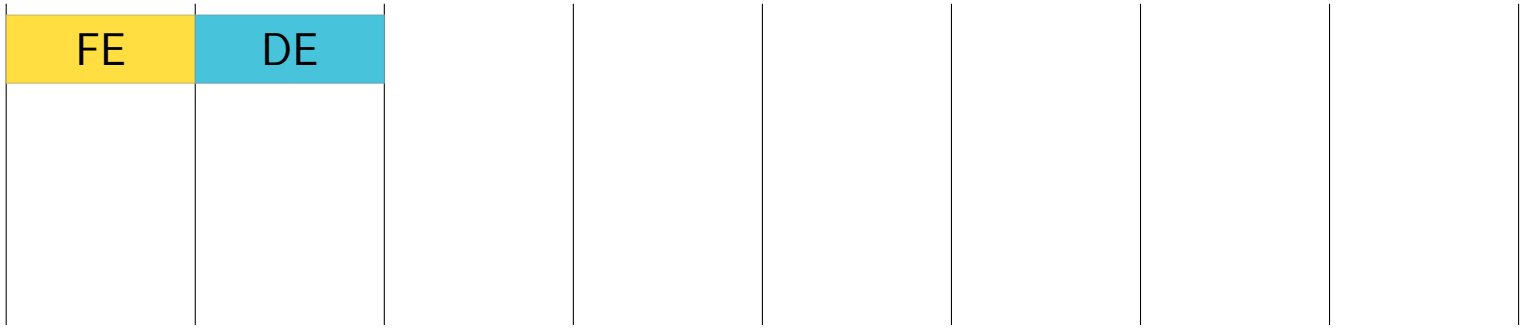

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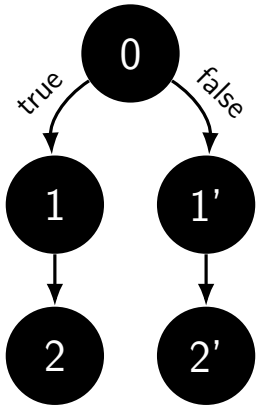


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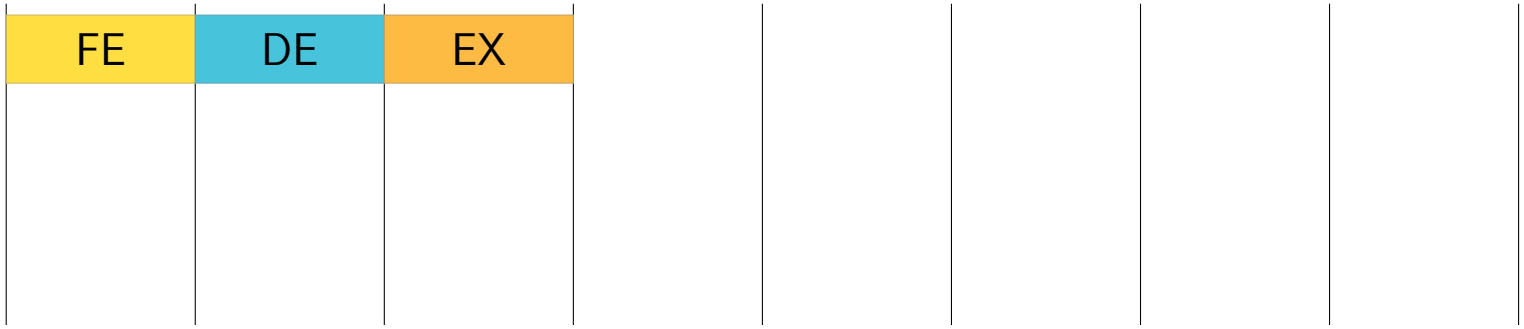

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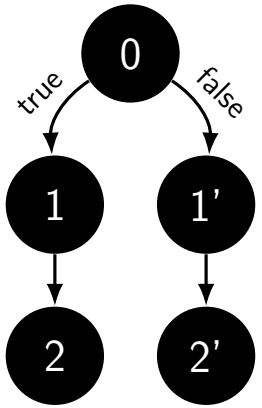

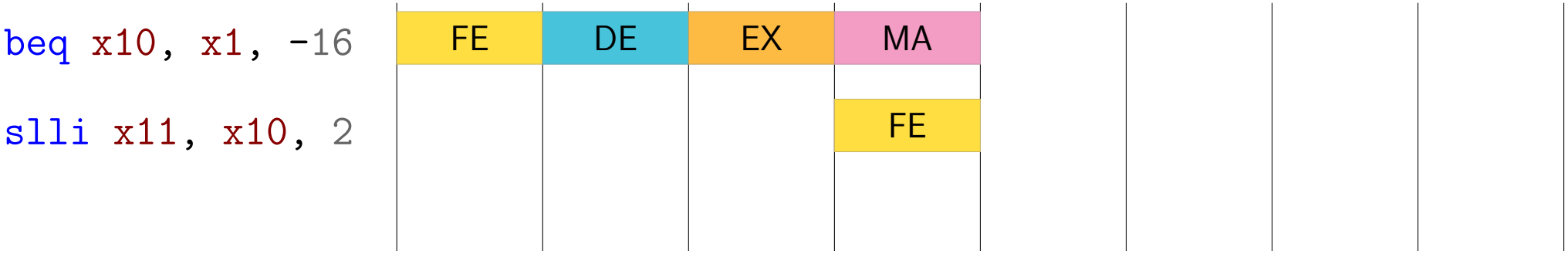

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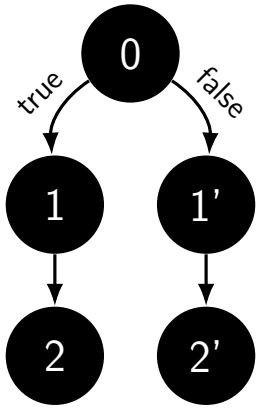

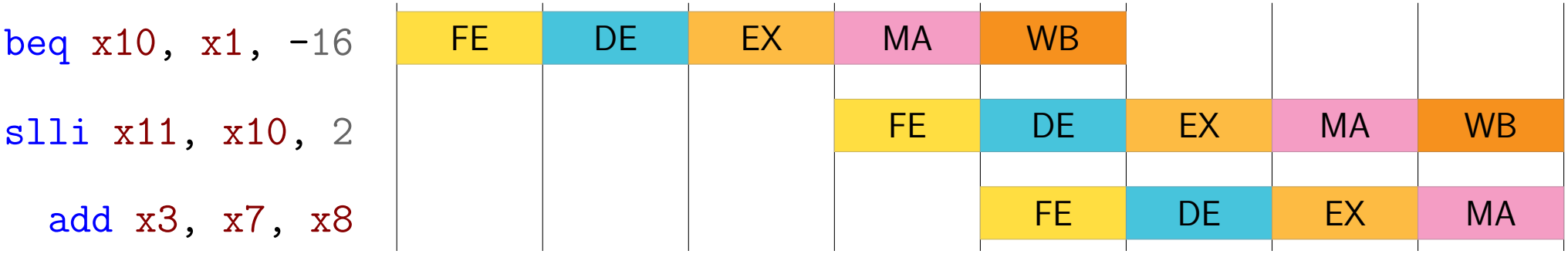

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Recap: IPC of 1 is ideal

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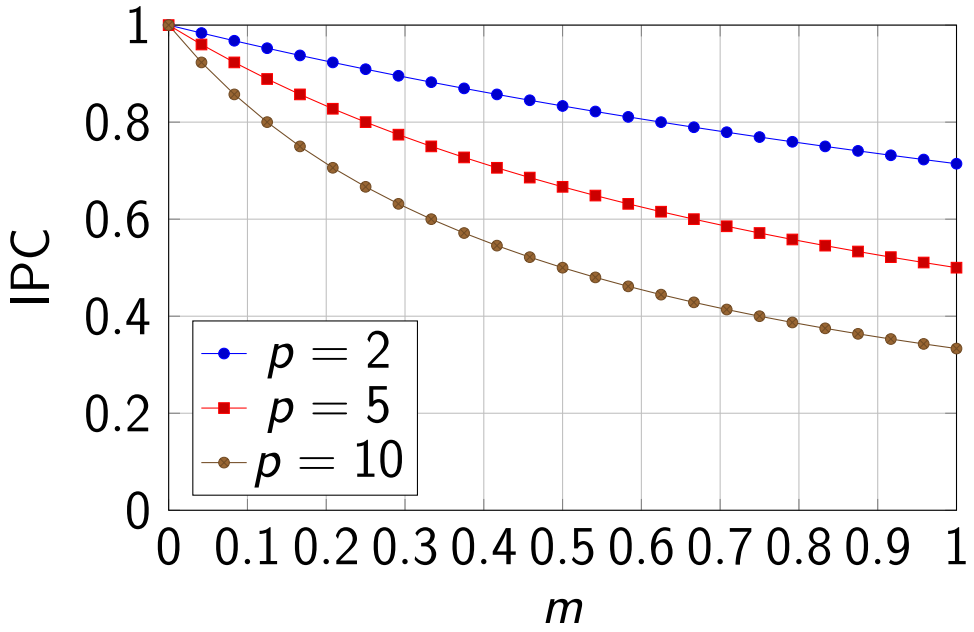

Reduce the Impact of Branches

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Avoid Branches

Replace branch instructions with other instructions

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Predict Branches

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Modify code, example **loop unrolling**

- Rewrite loops in repeating code sequences
- Reduces number of branches, but increases code size
- This is most often done by the compiler (inner loops, few iterations)

Loop Unrolling

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Example: 3 nested loops

```
for (int i=0; i<3; i++)
  for (int j=0; j<3; j++)
    for (int k=0; k<3; k++)
        Z[i][j] += X[i][k] * Y[k][j];
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Loop unrolling of most inner loop:

```
for (int i=0; i<3; i++)
  for (int j=0; j<3; j++)
    Z[i][j] += X[i][0] * X[0][j] + X[i][1] * X[0][1]
             + X[i][2] * X[2][j];
```


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Machine decision

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Machine decision

- Predict based on inspection of the instruction

Static Branch Prediction: Always

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Observation: Probability of branch taken is 60-70%

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Idea: Always predict the jump

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- 20% of instructions are branches

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- Misprediction penalty: 5 cycles (realistic for 11-15 stage pipeline)

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What is the IPC?

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What is the IPC?

$$\text{IPC} = \frac{1}{1 + 0.2 \cdot (1 - 0.7) \cdot 5} = \frac{1}{1.3} = 0.77$$

Static Branch Prediction: Direction

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Look closer at branches

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Observation: Differences by branch direction

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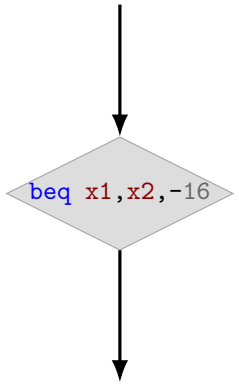
Backward branch



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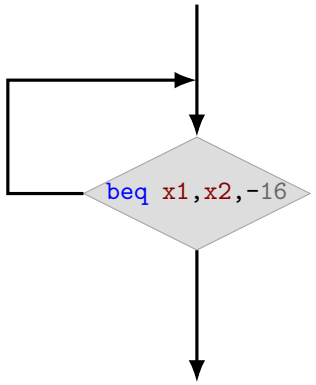

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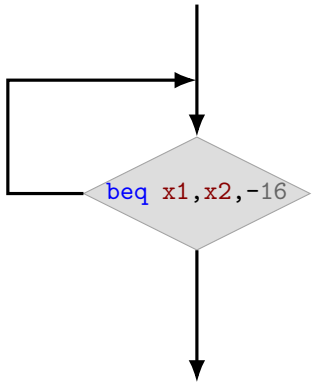

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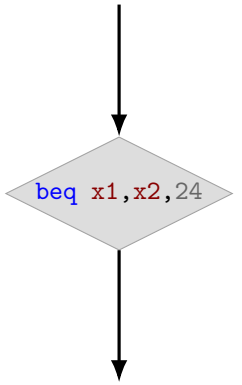

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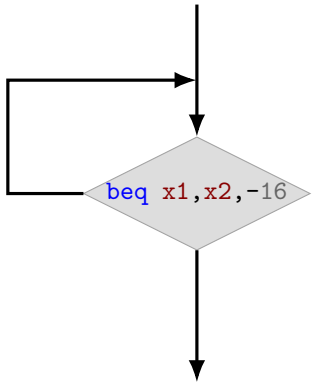

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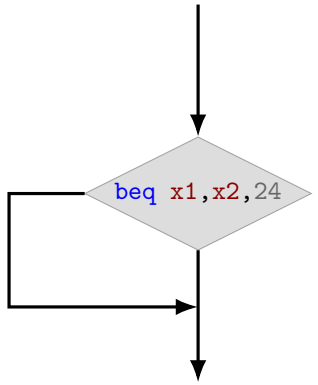

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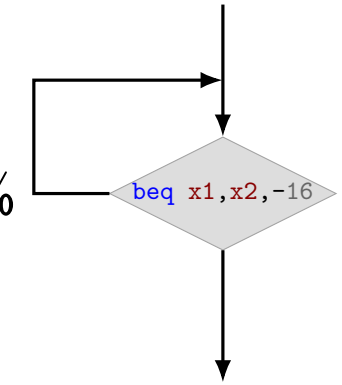
ca. 90%



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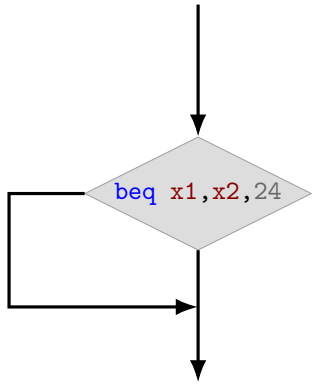

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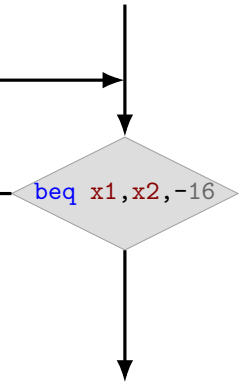
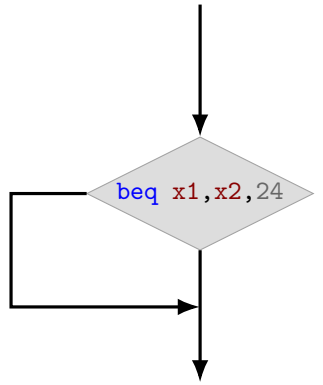


Forward branch

ca. 50%



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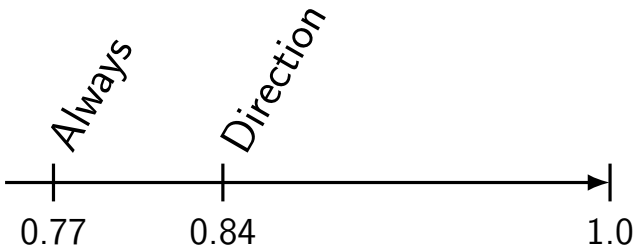

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  If a branch was taken recently, it will probably be taken again (loops, etc.)

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Based on **correlations**

- *Temporal correlation*
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- *Spatial correlation*
  Branches on an execution path will probably behave similarly with each execution of the path

Dynamische Branch Prediction: 1-bit Predictor

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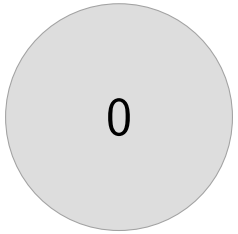
Idea: Consider last branch decision



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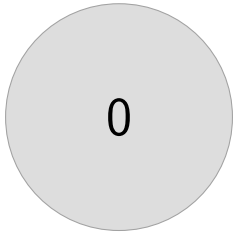
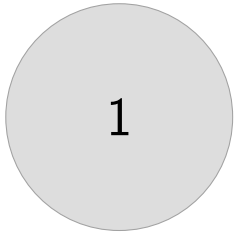
1 bit counter/state machine





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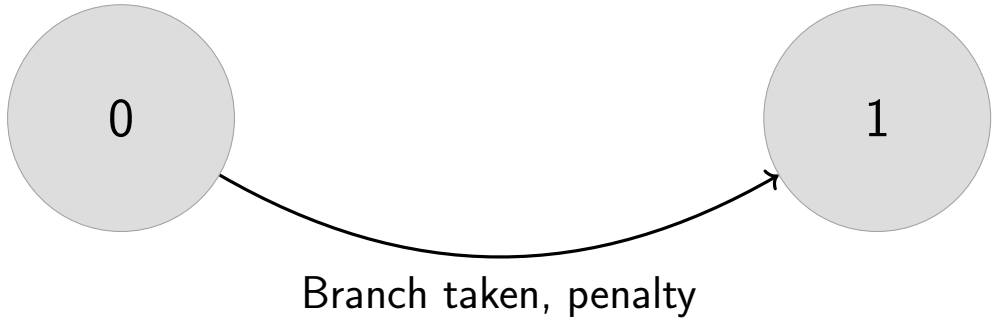

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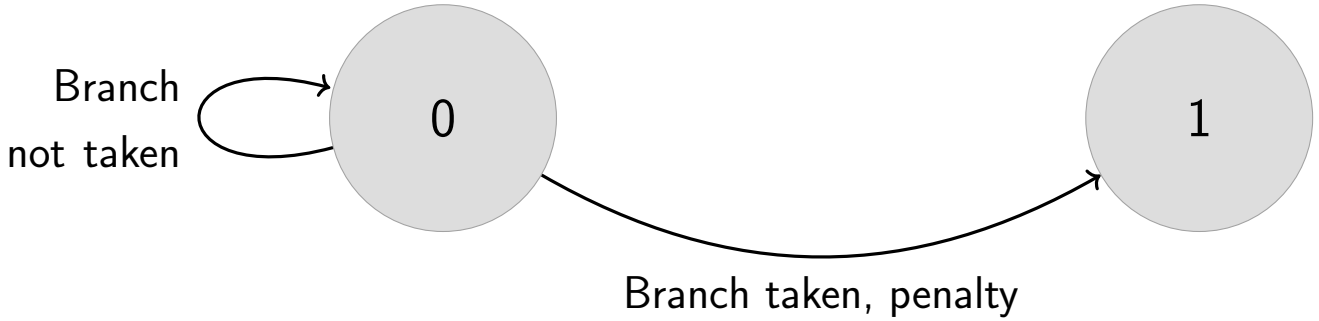

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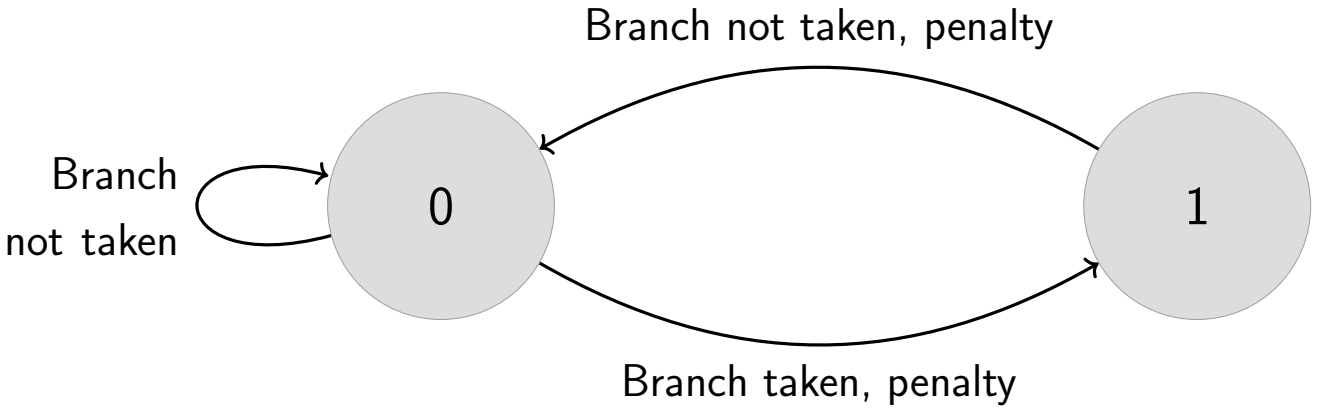

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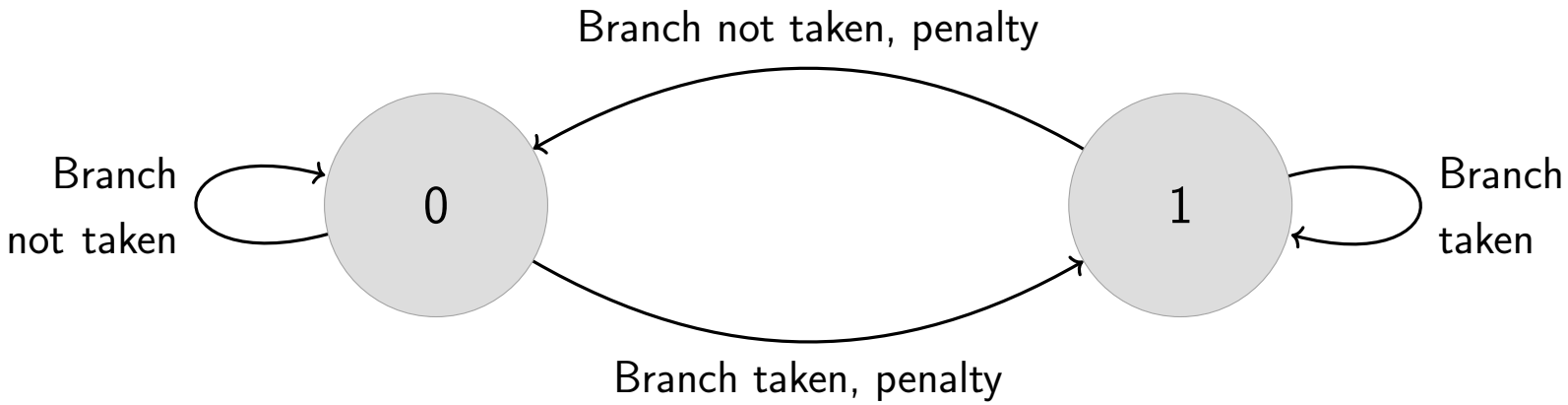

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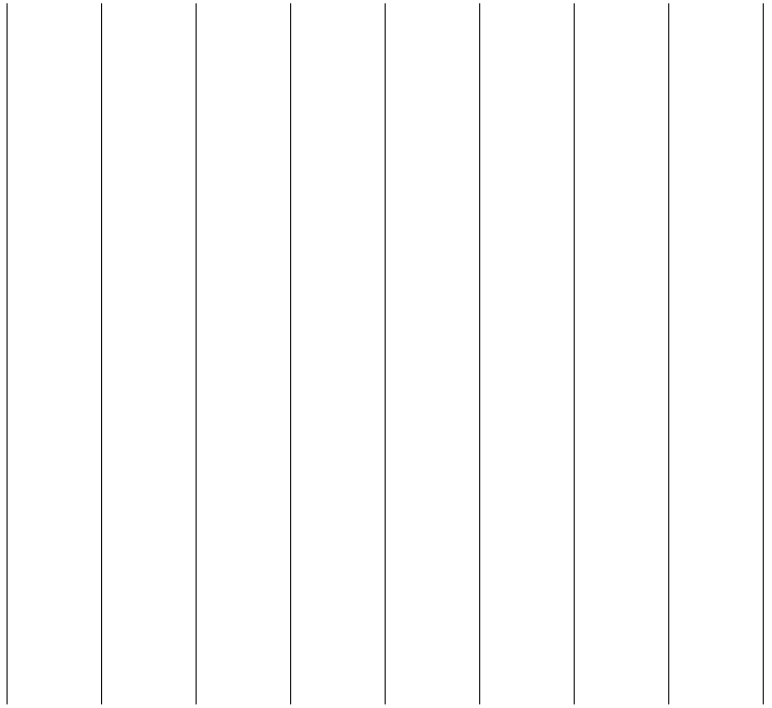

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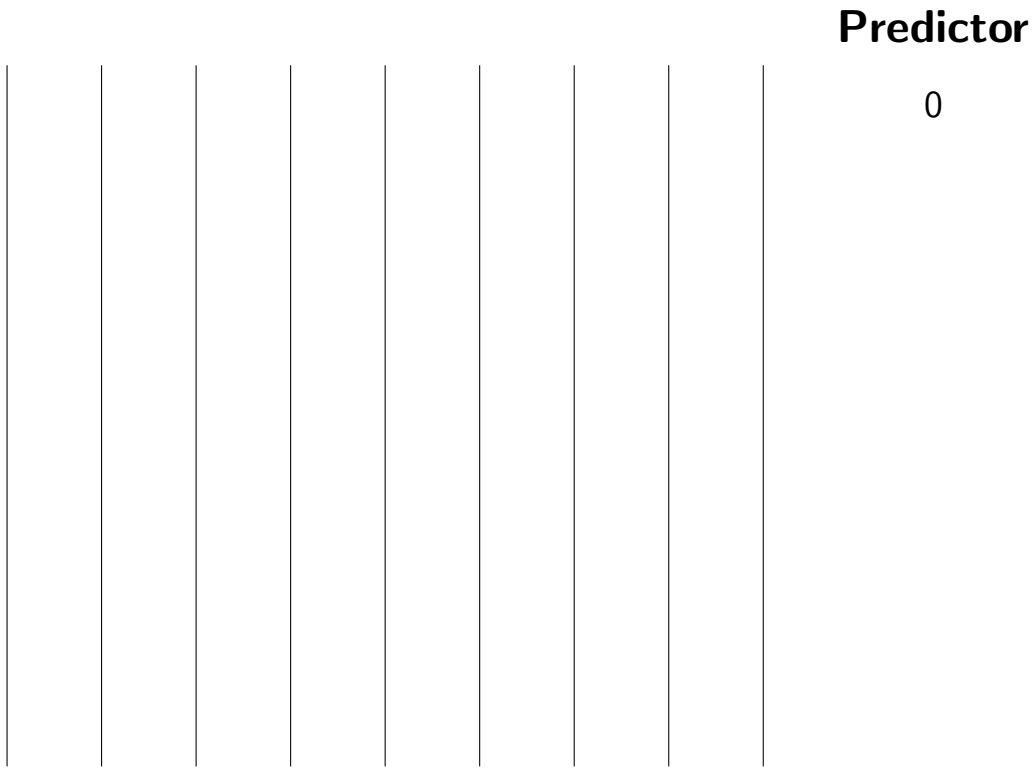

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	Predictor
`beqz x10, 24`	0

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PC		Predictor
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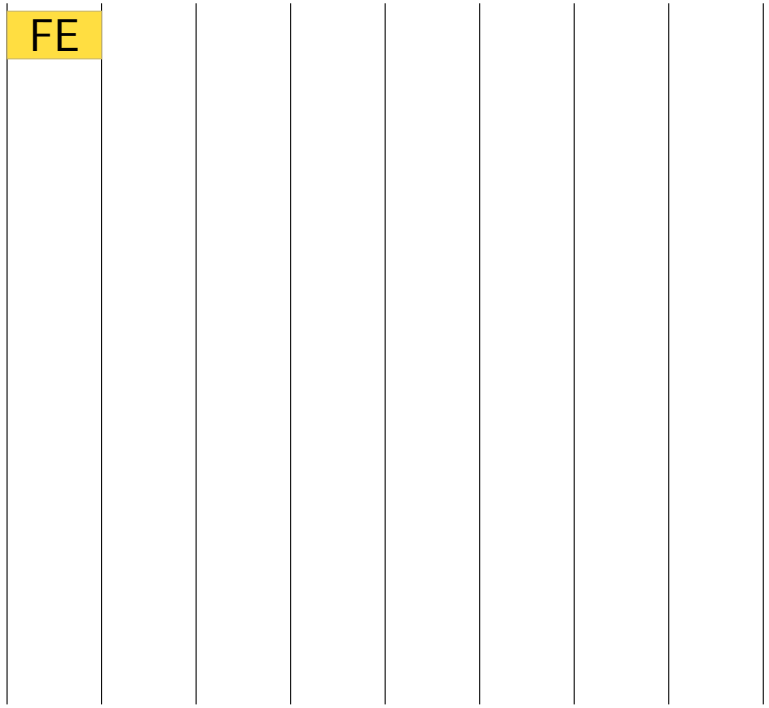

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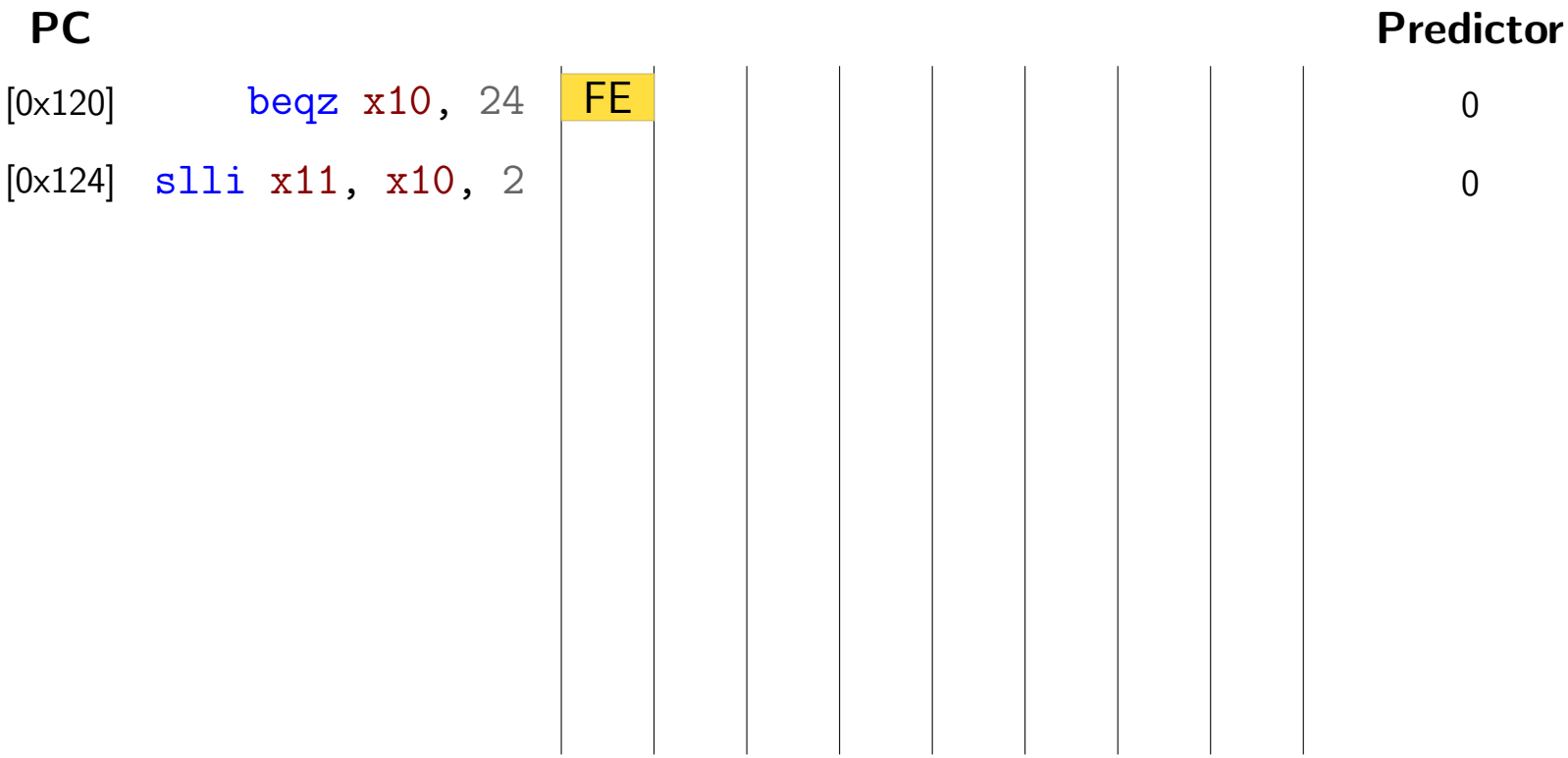

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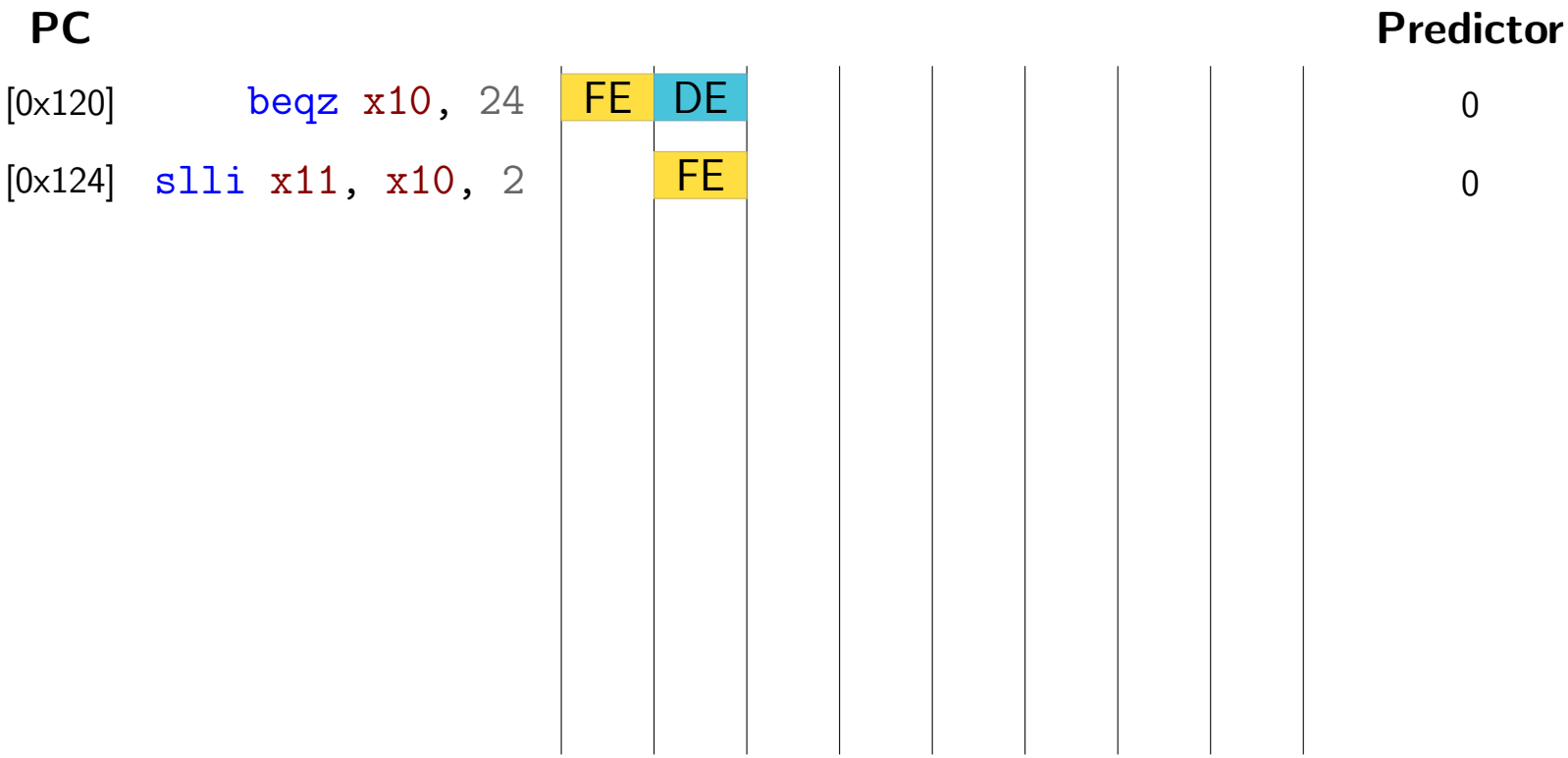

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PC		Predictor
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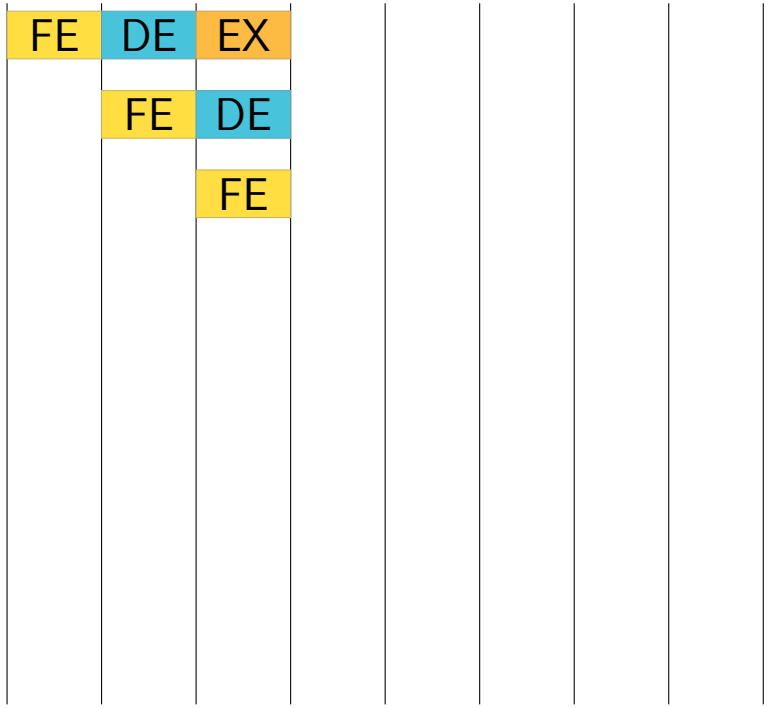
[0x128]	`add x11, x11, x8`	0



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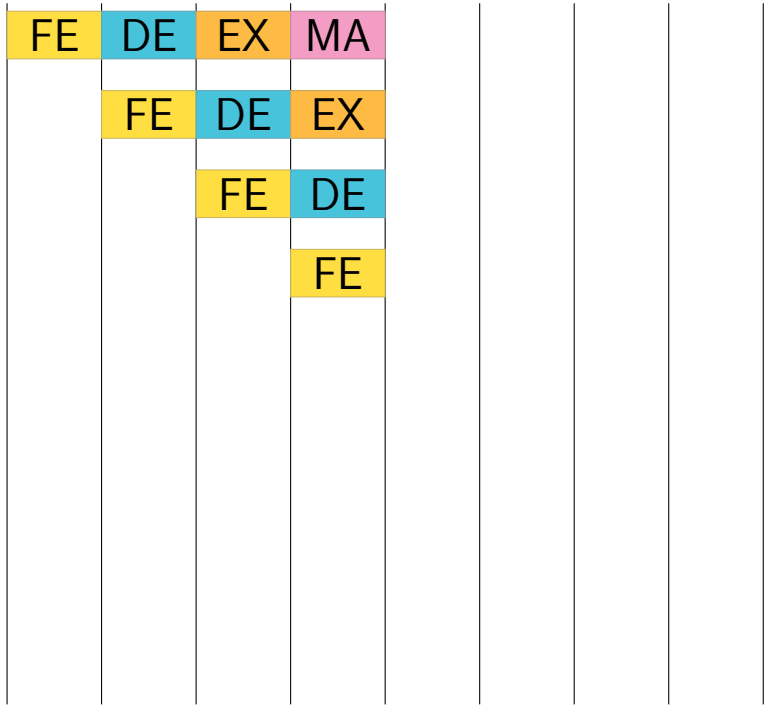
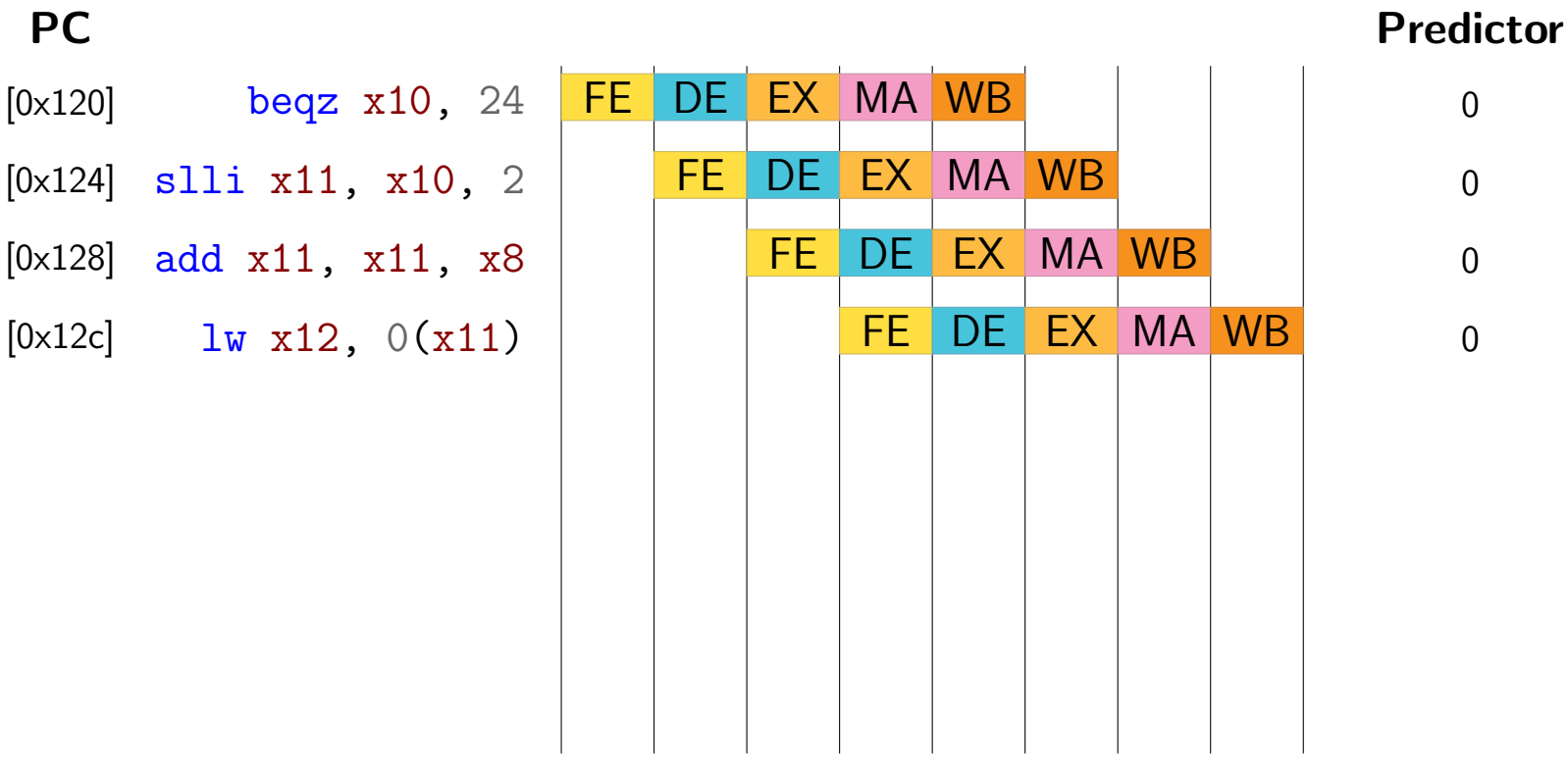
[0x12c]	`lw x12, 0(x11)`	0



1-bit Predictor: Example



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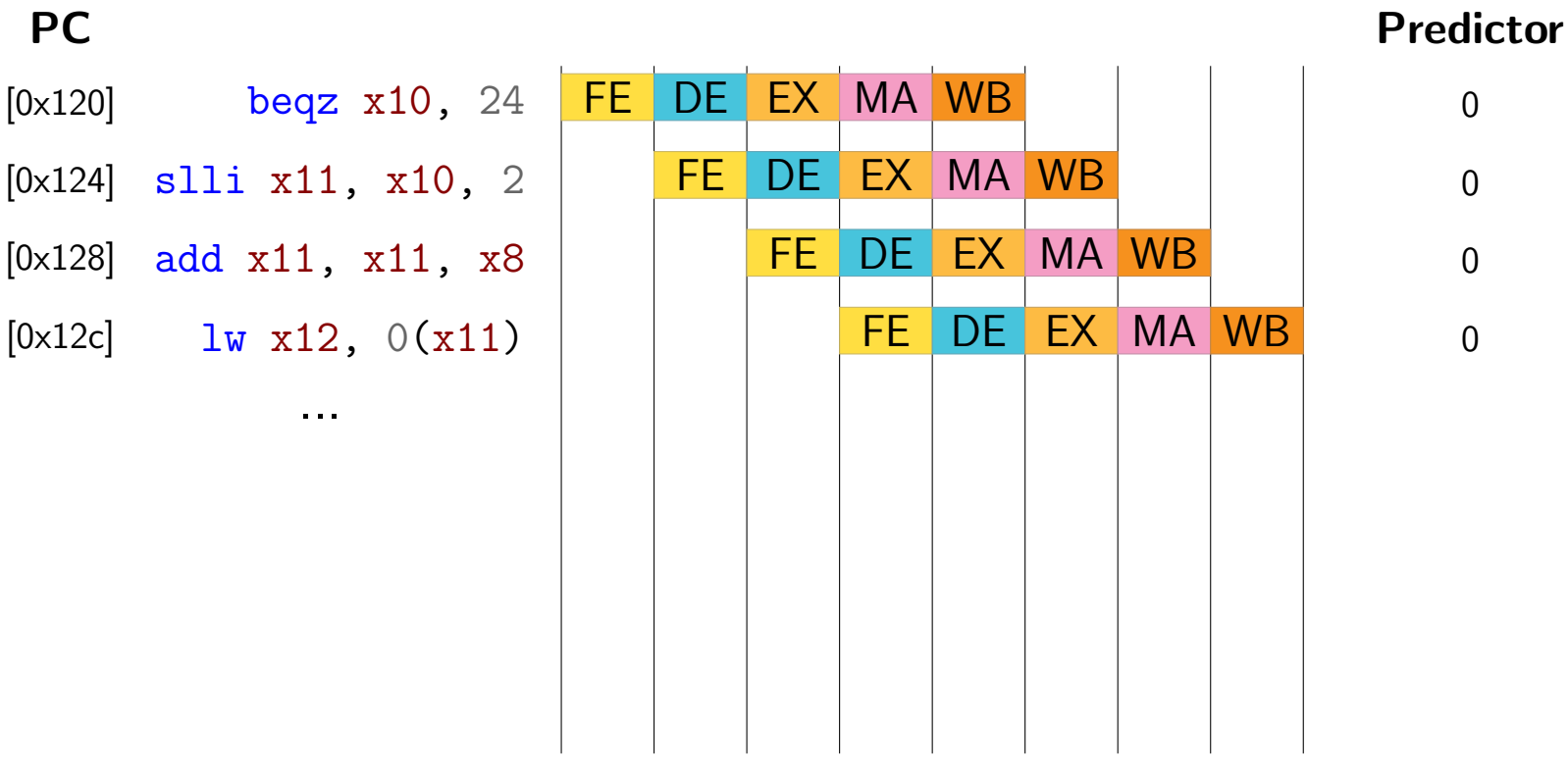

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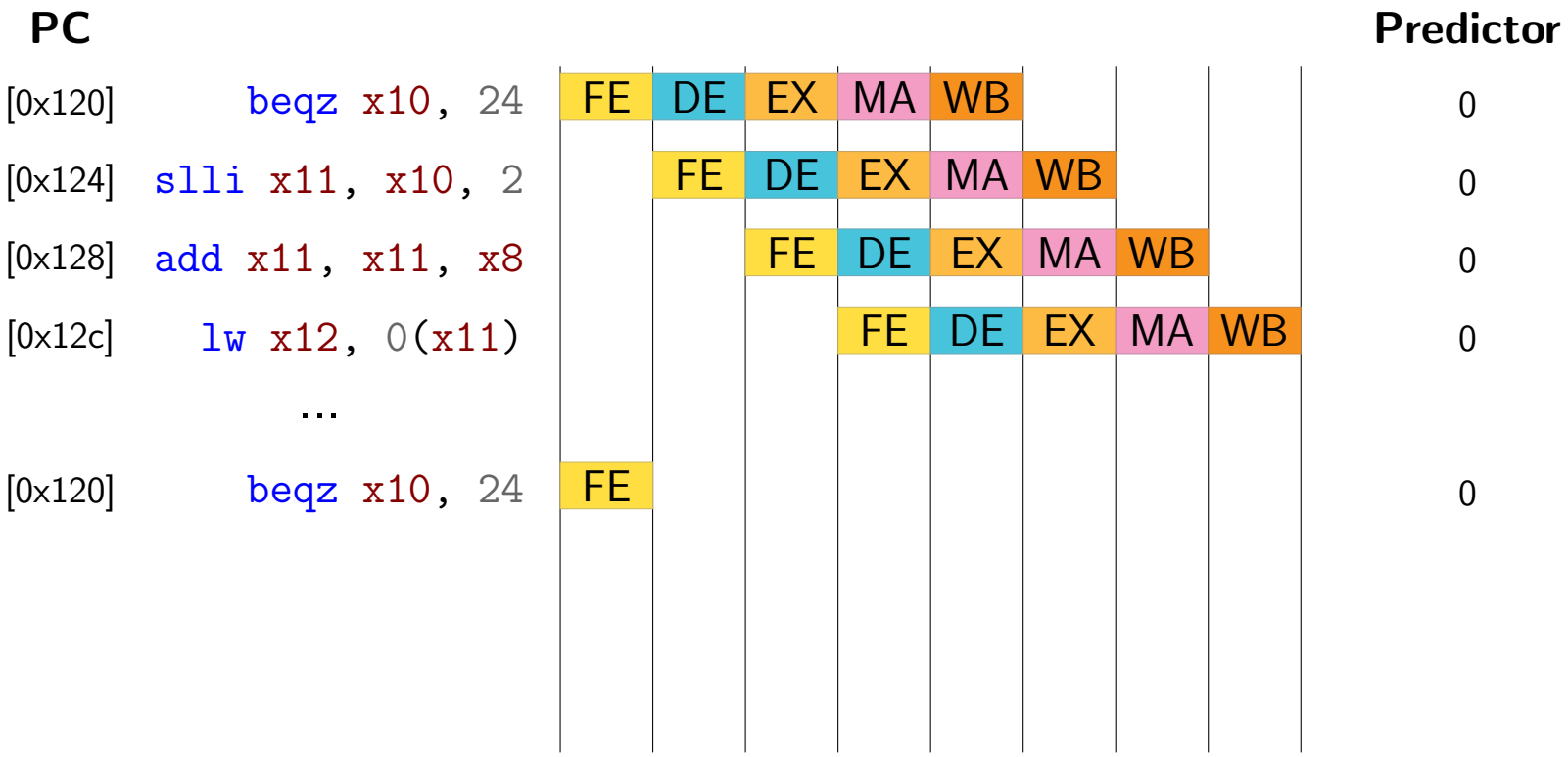

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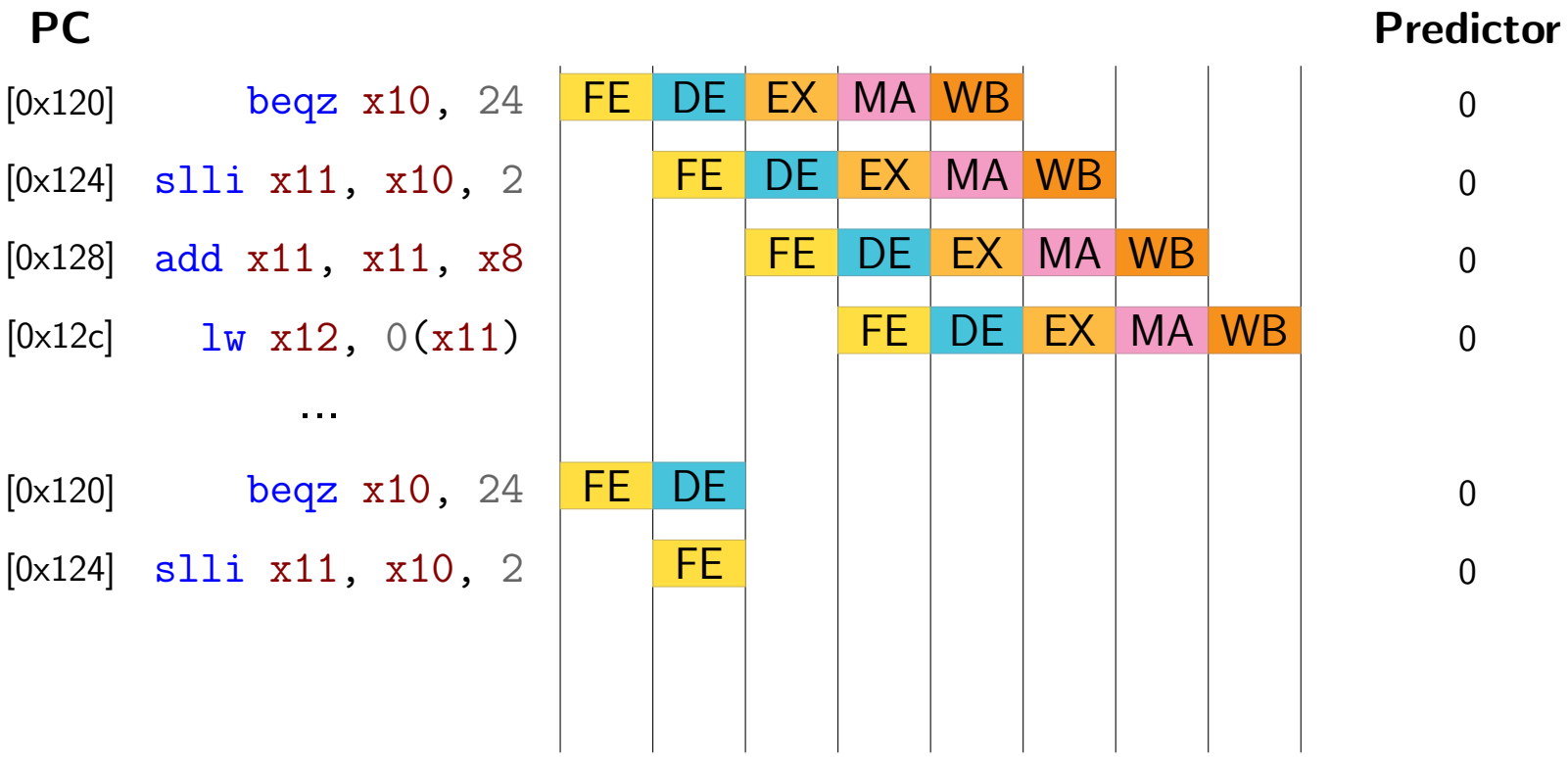

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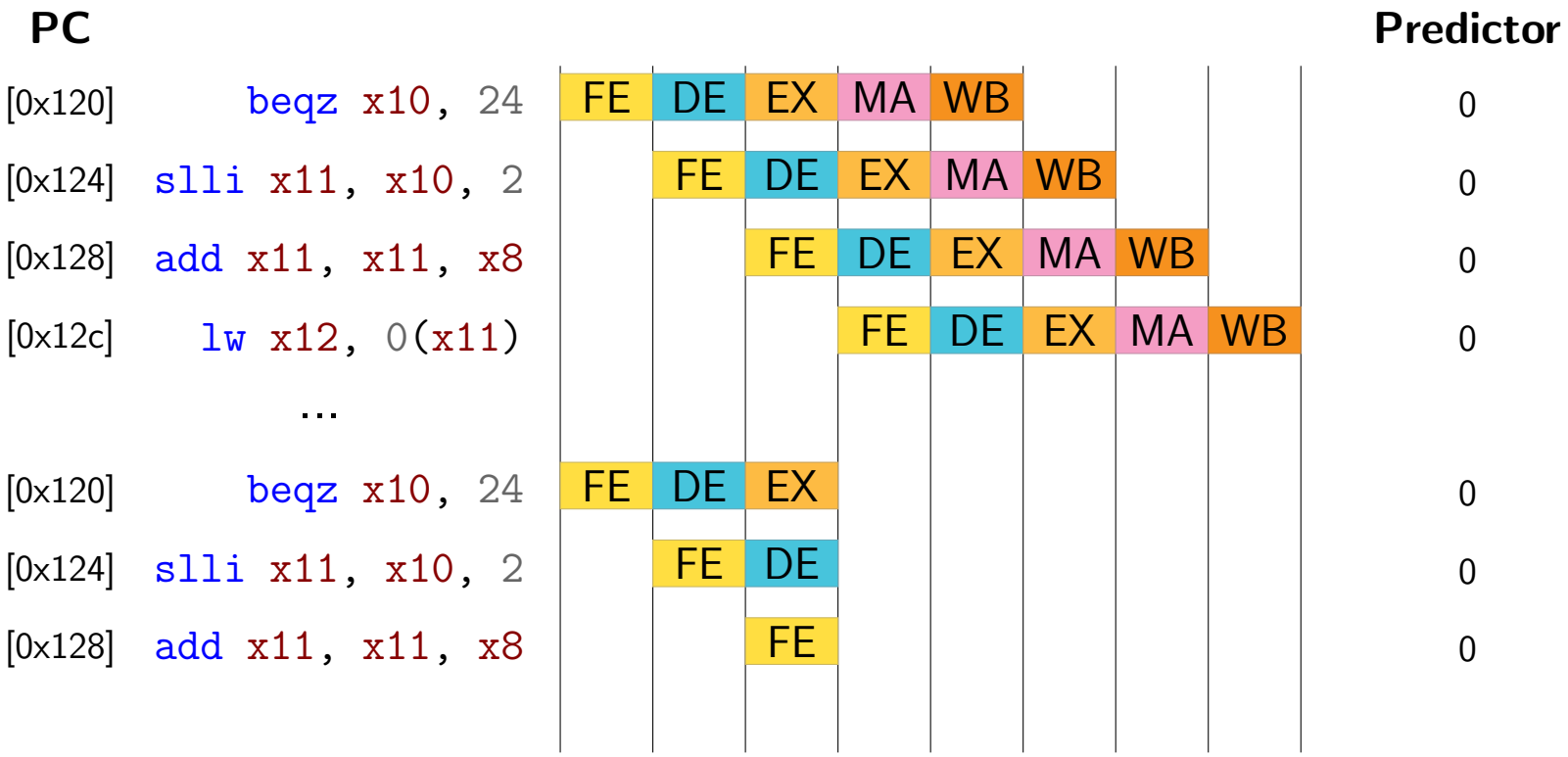

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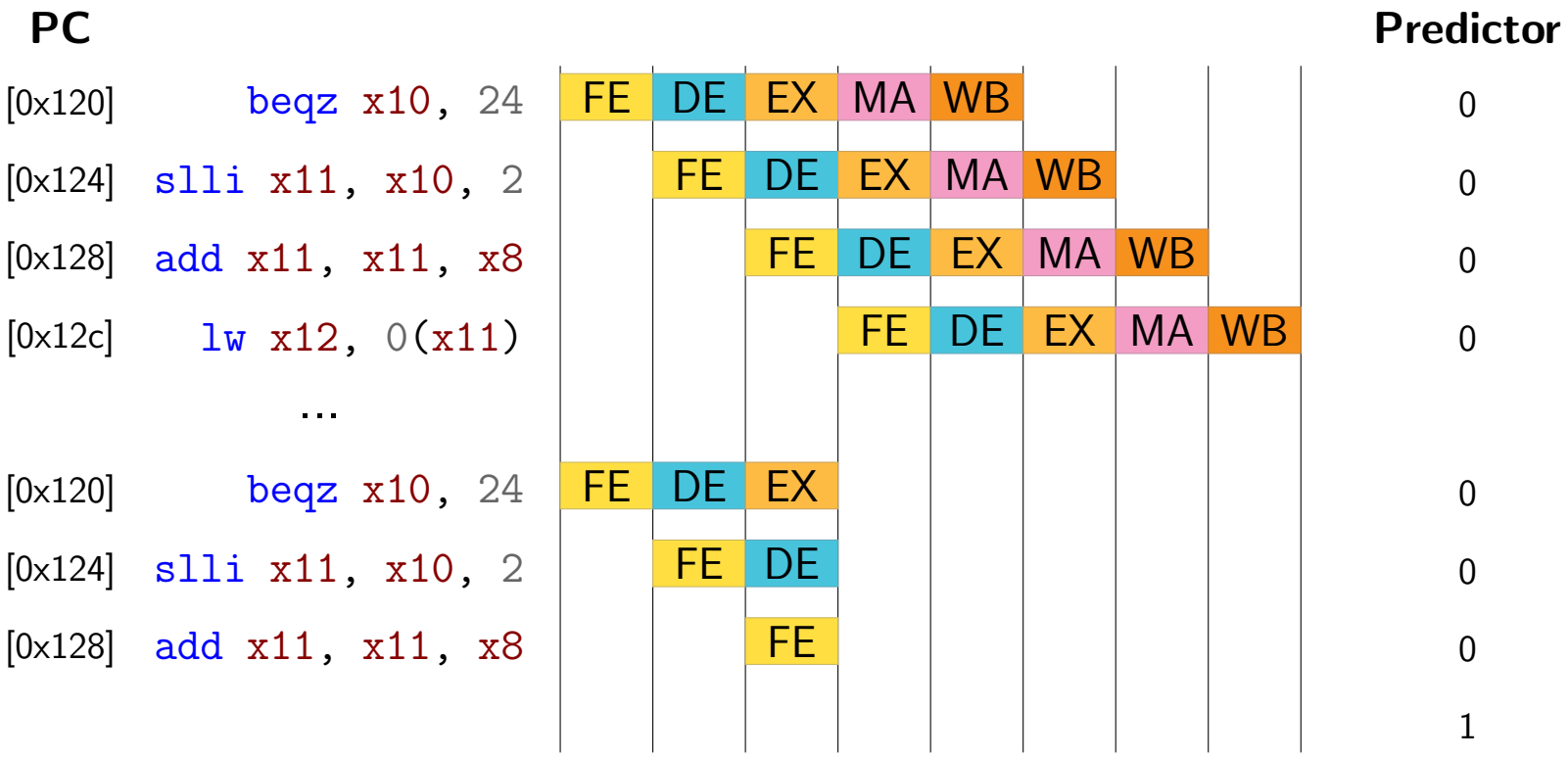

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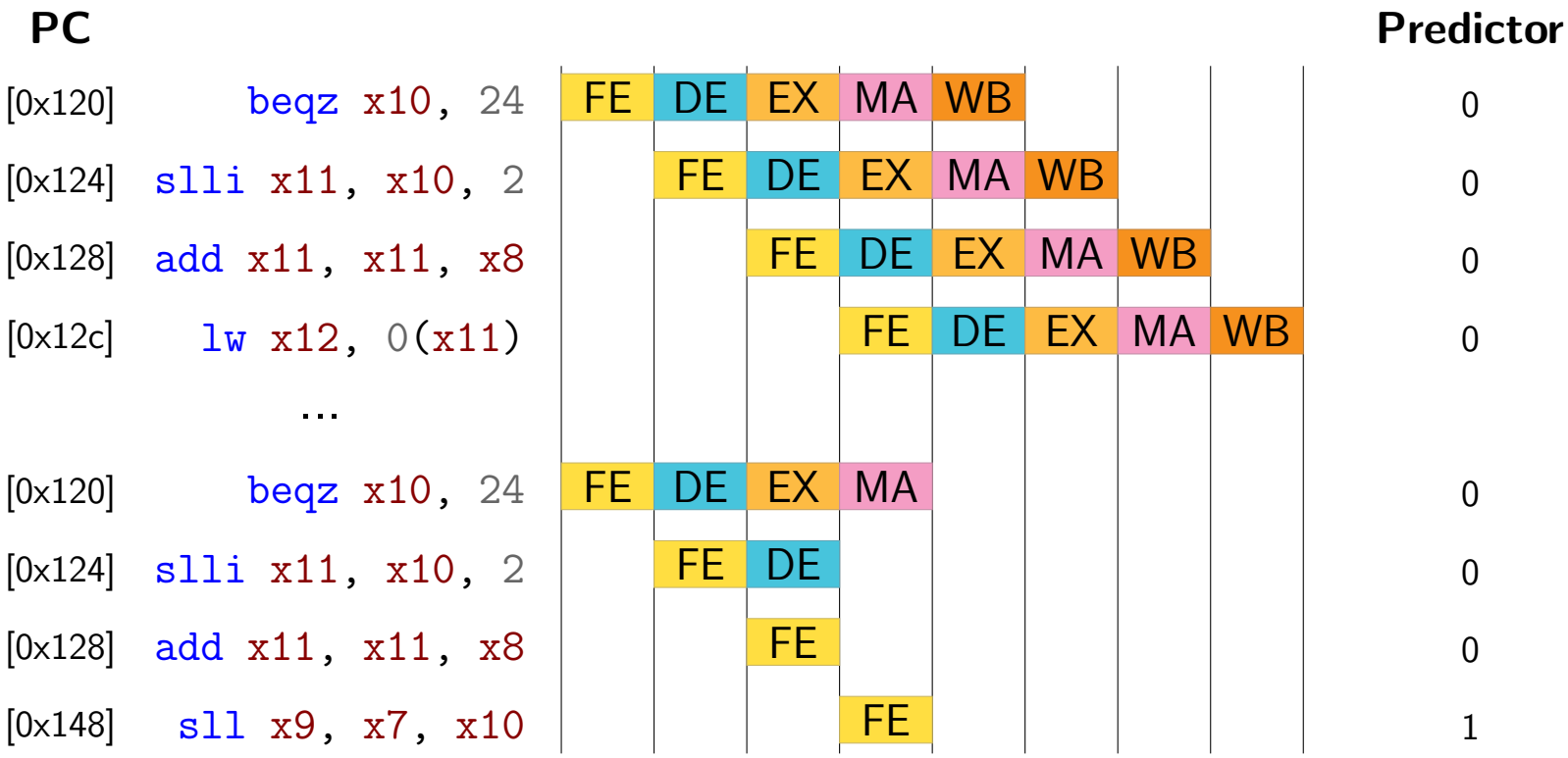

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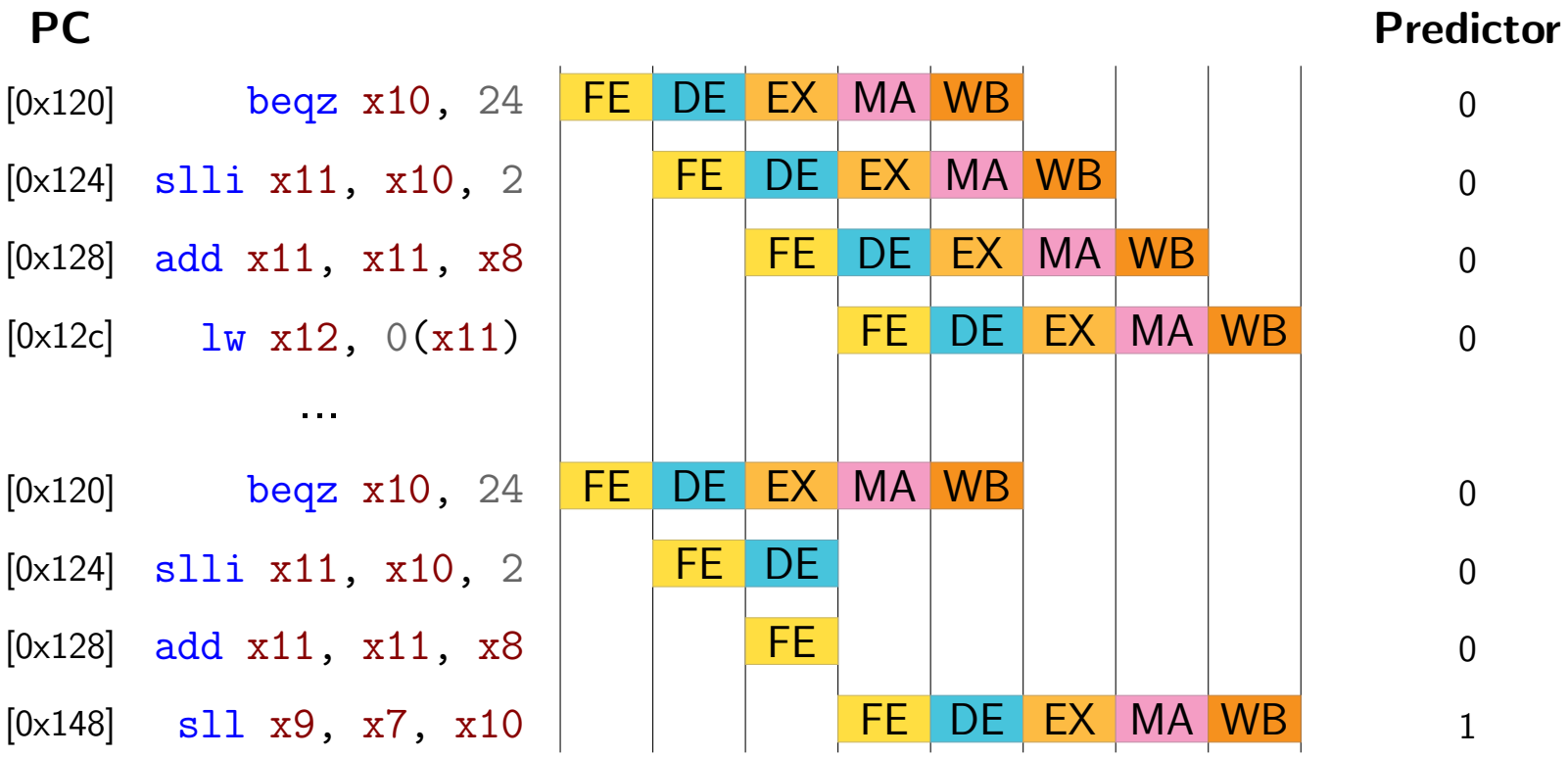

1-bit Predictor: Multiple Branches

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Single bit to track all branches

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Problem: Multiple branches

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Single bit to track all branches

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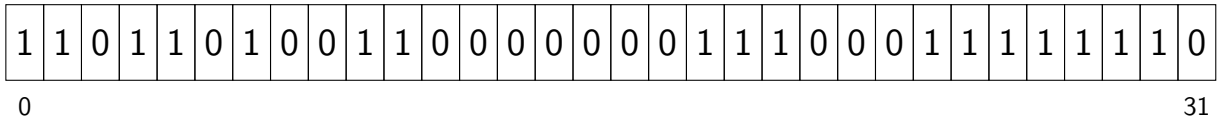
- Nested loop, control structures, function calls
- Share the same predictor and mispredicts

Ideal solution: One predictor per branch

- No interference, exclusive resource
- **but**: Need as many predictors as potential branches

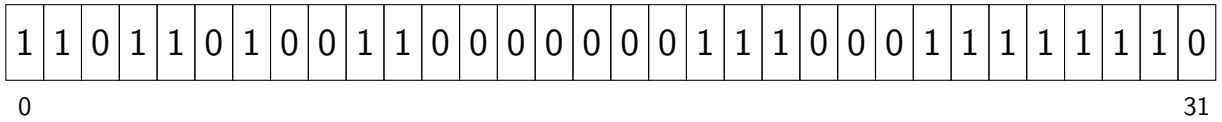
Real solution: Use multiple predictors

Multiple 1-bit Predictors



Multiple 1-bit Predictors

Selection of multiple predictors based on program counter



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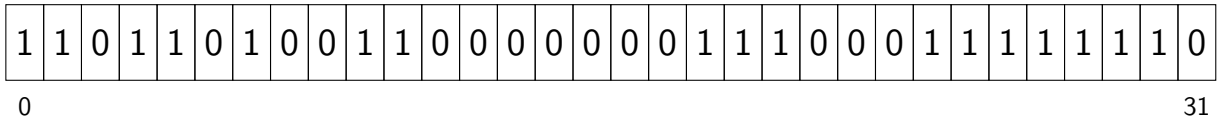
Selection of multiple predictors based on program counter

Which portion of program counter?

0x0F00138 = 00001111000000000000000100111000



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Which portion of program counter?

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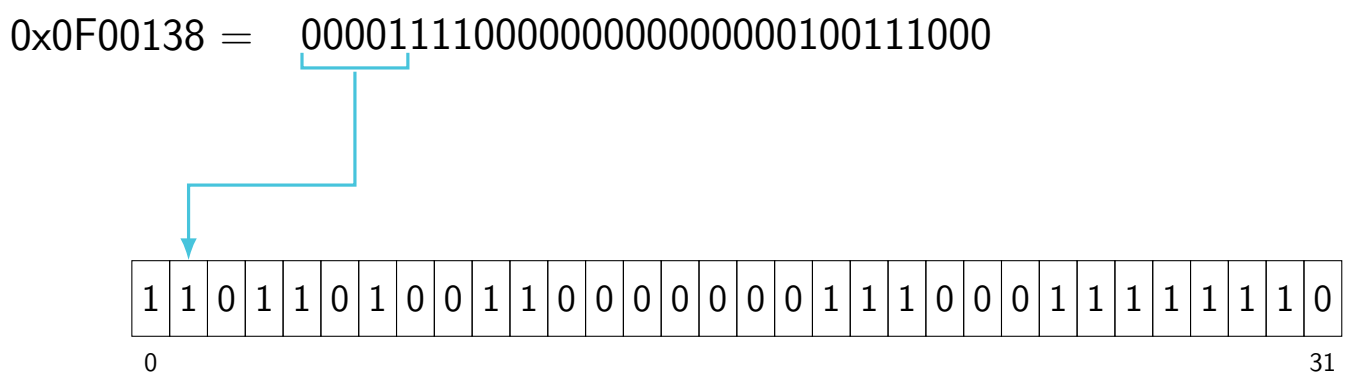

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Selection of multiple predictors based on program counter

Which portion of program counter?

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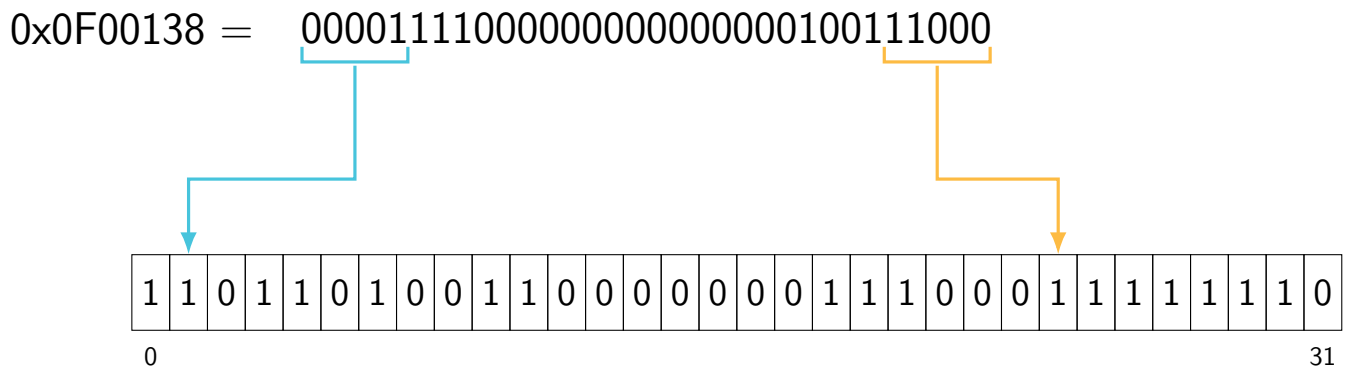
- Least significant bits are problematic: 3 out of 4 predictors never addressed



Multiple 1-bit Predictors

Selection of multiple predictors based on program counter

Which portion of program counter?

- Most significant bits are problematic: aliasing of adjacent branches
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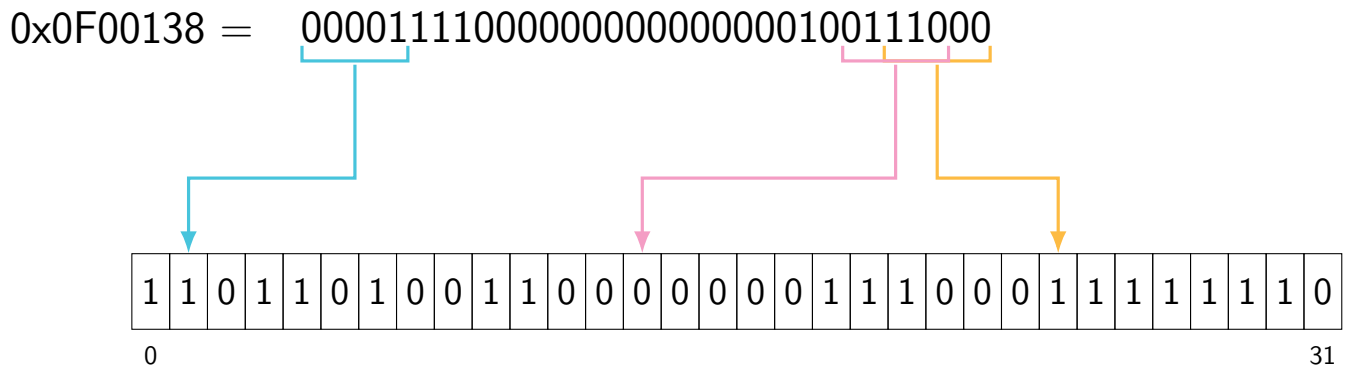
- Leat signigicant, *non-static* bits: adjacent branches map to different predictors



1-bit Predictor: IPC

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Observation: 85% accuracy

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$$\text{CPI} = 1 + 0.2 \cdot (1 - 0.85) \cdot 5 = 1.15$$

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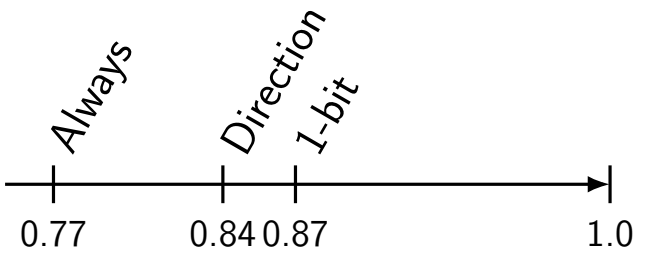

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Consider branch taken over time for a particular branch (1/0 branch taken/not taken)

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Example: Inner loop

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     do_something(x,y);
```

is compiled to:

```
       li s0, 1024
xloop: li s1, 4
yloop: mv a0, s0
       mv a1, s1
       jal ra, do_something
       addi s1, s1, -1
       bnez s1, yloop
       addi s0, s0, -1
       bnez s0, xloop
```


1-bit Predictor: Limitations

Consider branch taken over time for a particular branch (1/0 branch taken/not taken)

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- Branch decisions of y loop (take loop again): 1110111011110...

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- Predicted: 111101110111...

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Consider branch taken over time for a particular branch (1/0 branch taken/not taken)

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- Branch decisions of y loop (take loop again): 111011101110...
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1-bit Predictor: Limitations

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Example: Inner loop

- Branch decisions of y loop (take loop again): 111011101110...
- Predicted: 111101110111...
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Outliers lead to double mispredict

How can we suppress this behavior?

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for (x = 1024; x > 0; x--)
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2-bit Predictor

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Approach: Make robust against "outliers" (filter)

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- *Saturating 2-bit counter*

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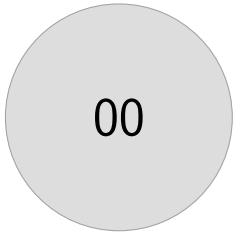

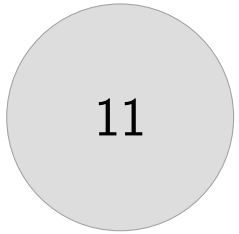

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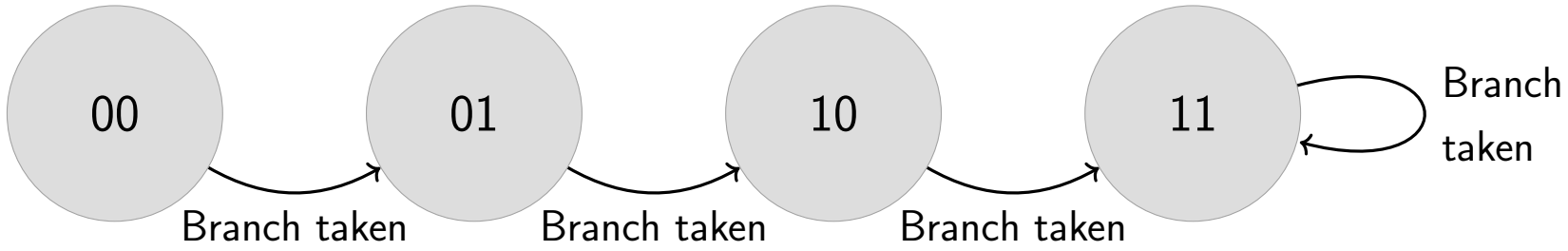

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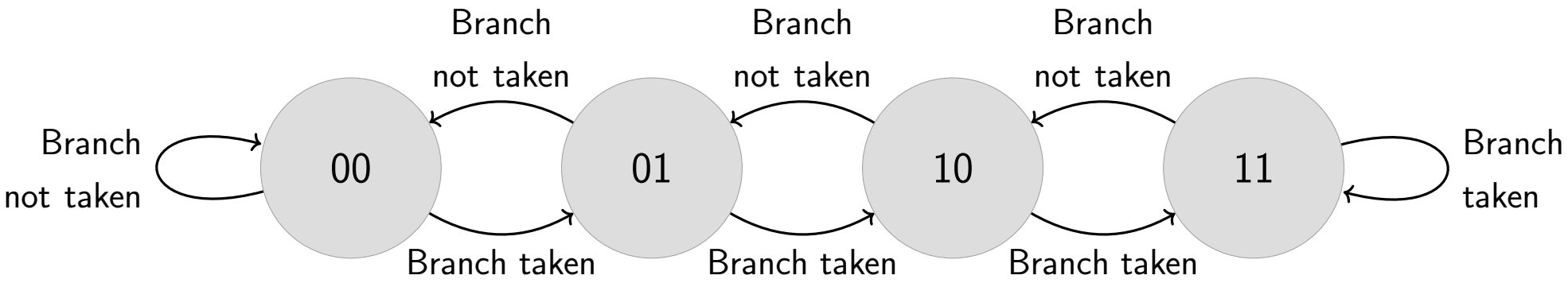

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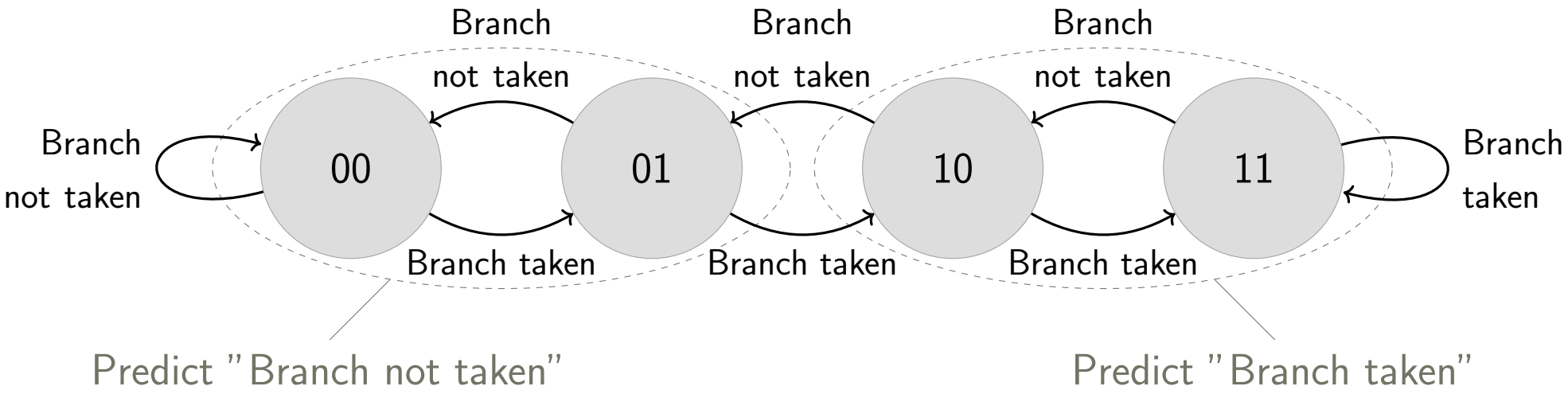

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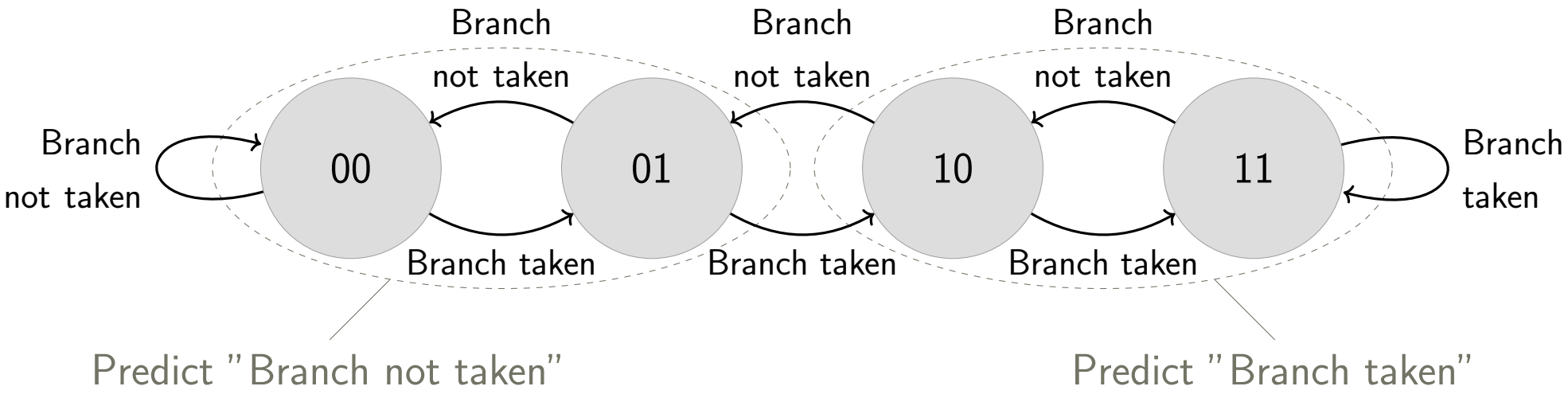

When do we get a penalty?

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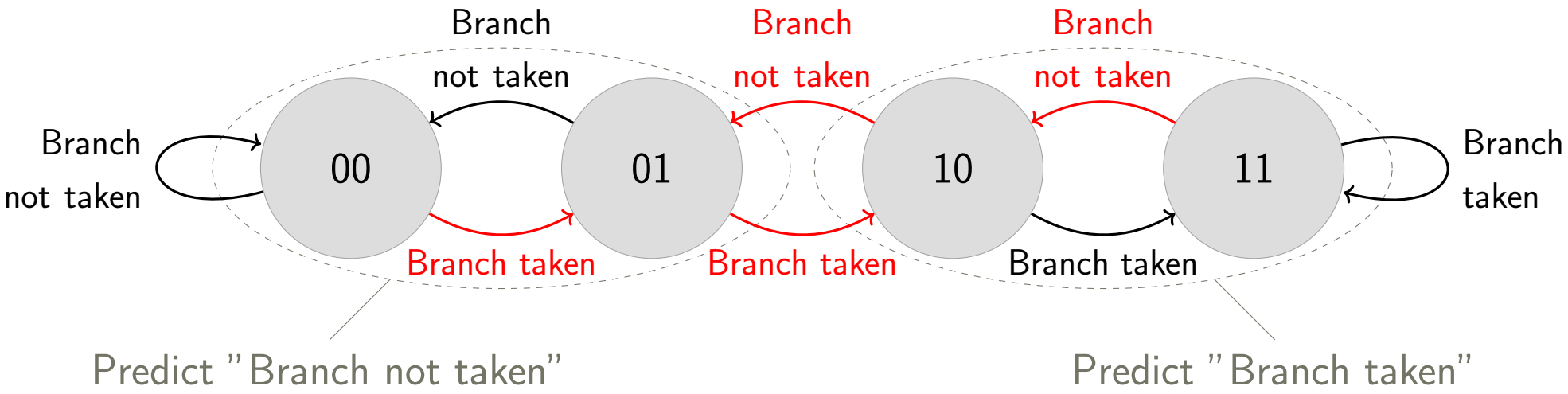

When do we get a penalty?

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Comparison to 1-bit predictor, example with nested loop

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for (x = 1024; x > 0; x--)
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2-bit Predictor: Improvement

Comparison to 1-bit predictor, example with nested loop

Branch taken?

1-bit

state (0)

predict

2-bit

state (01)

predict

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state 0

predict 0

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Branch taken?		1
1-bit	state	0
	predict	0
2-bit	state	01
	predict	0

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	predict	0↯
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state (0) (1)

predict 0↯

2-bit

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Comparison to 1-bit predictor, example with nested loop

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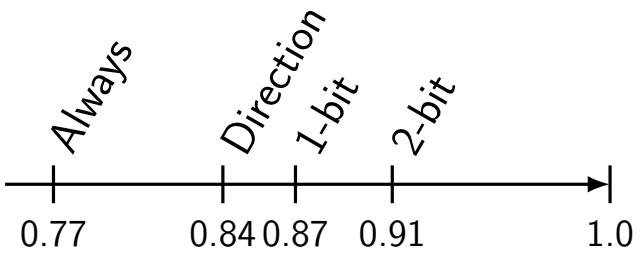

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- Recap: Nested loop iterations: 111011101110...
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Can we incorporate this regularity?

2-Way Adaptive Predictor

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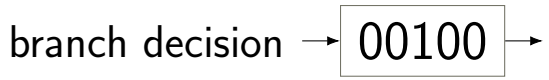
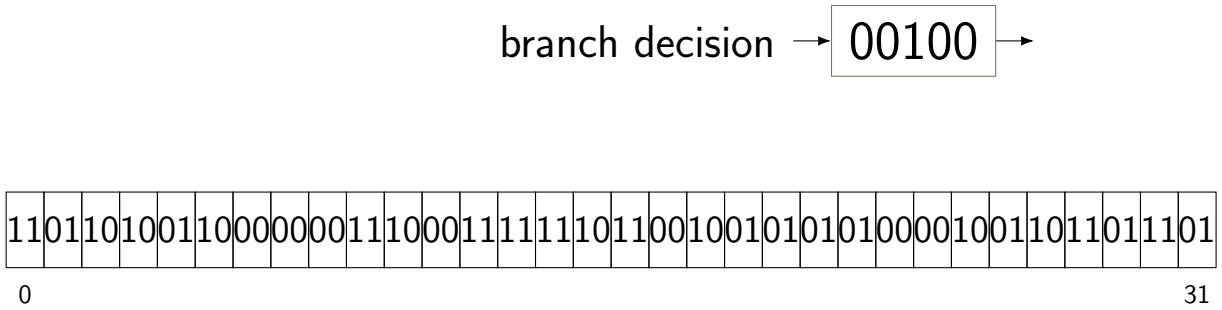
Save the last branch decisions



2-Way Adaptive Predictor

Save the last branch decisions

Select predictor based on history

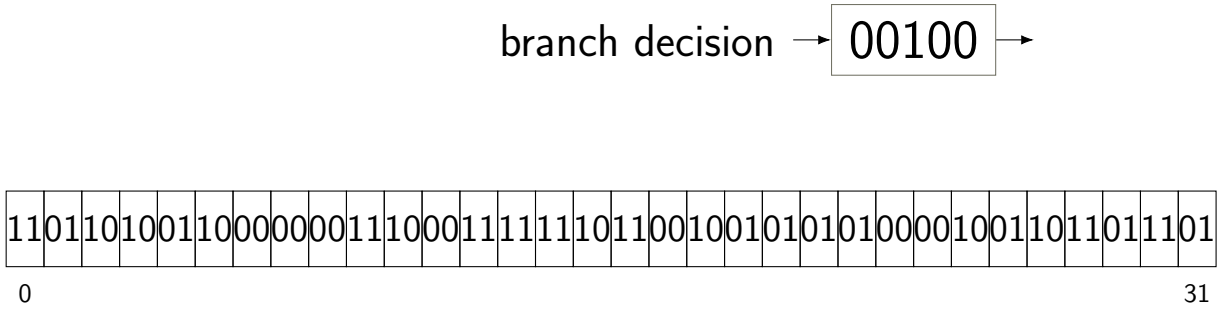


2-Way Adaptive Predictor

Save the last branch decisions

Select predictor based on history

- Before: Selection based on PC

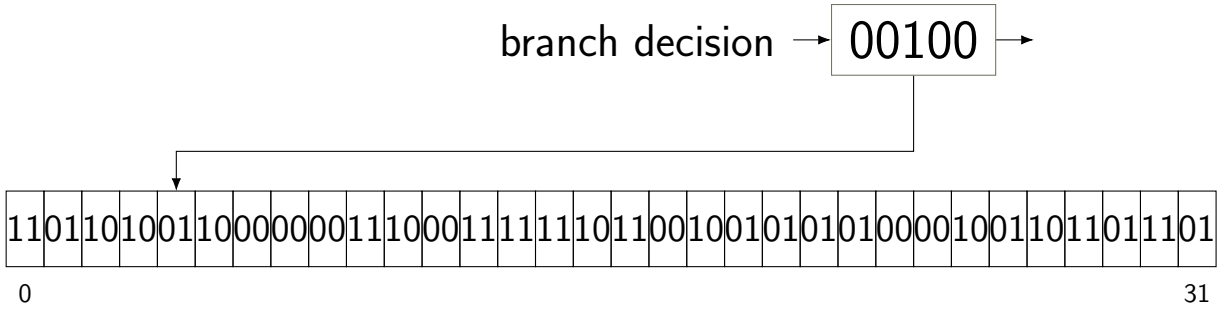


2-Way Adaptive Predictor

Save the last branch decisions

Select predictor based on history

- Before: Selection based on PC
- Now: Use history of most recent branch decisions



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Select predictor based on history

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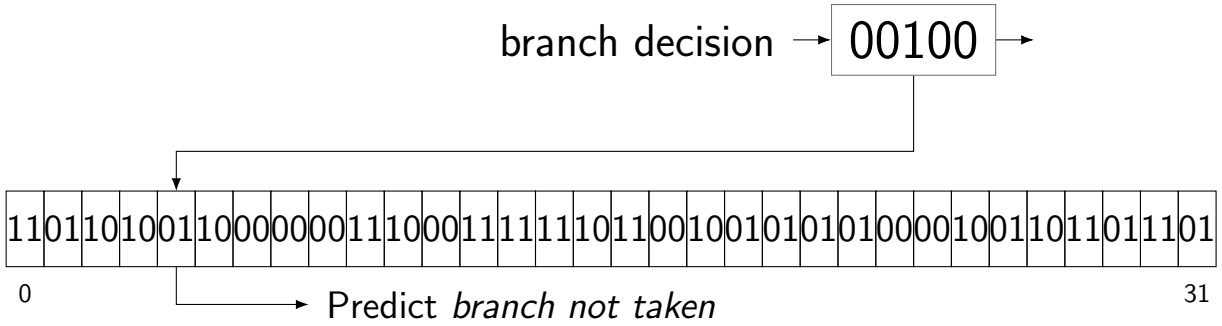
The *actual predictor* ("2nd way") stays the same (for example 2-bit predictor)



Adaptive Predictor: Example

```
        li s0, 1024
xloop:  li s1, 4
yloop:  mv a0, s0
        mv a1, s1
        jal ra, do_something
        addi s1, s1, -1
branch y →bnez s1, yloop
        addi s0, s0, -1
branch x →bnez s0, xloop
```

Adaptive Predictor: Example

5 bit of history (init: 00000), 32 Predictors

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History 0 0 0 0 0

Branch

line

taken

Predictor

id

state

predict

new state

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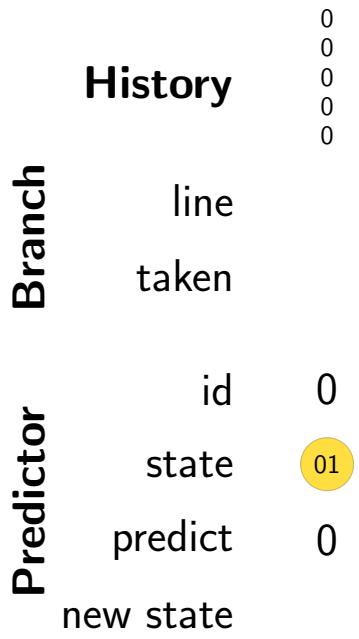


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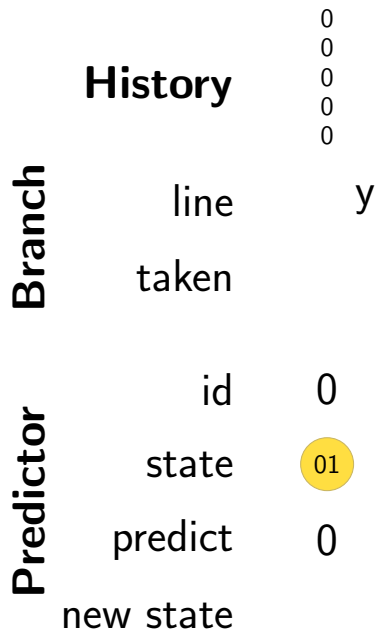


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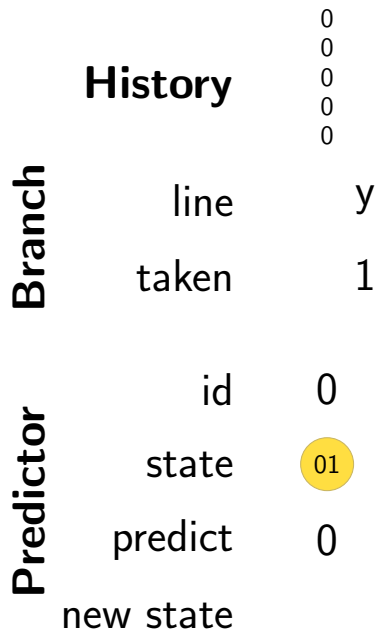


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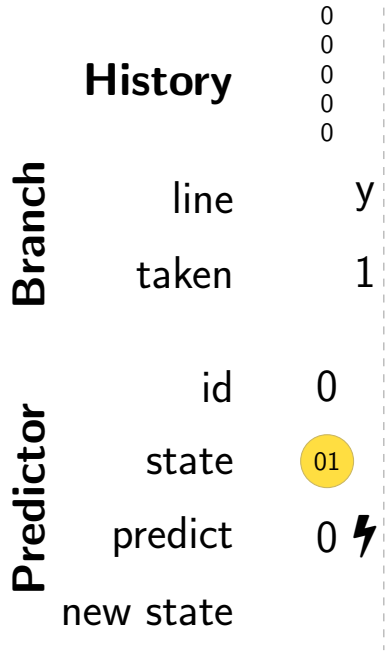


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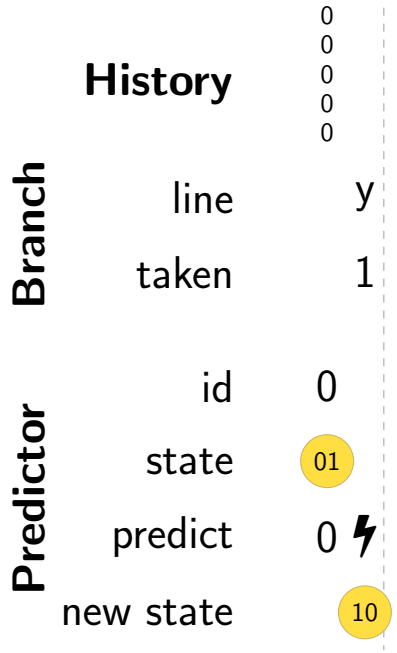


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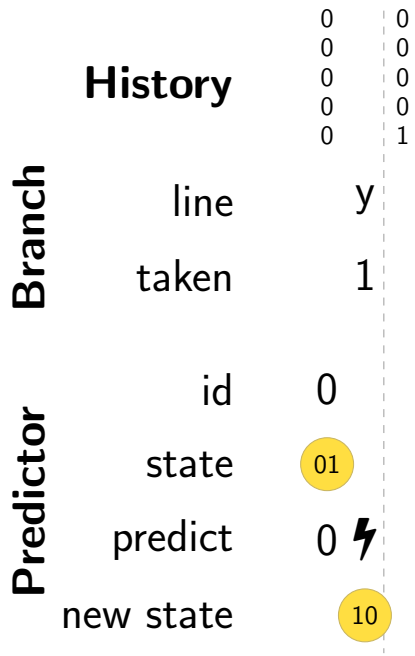


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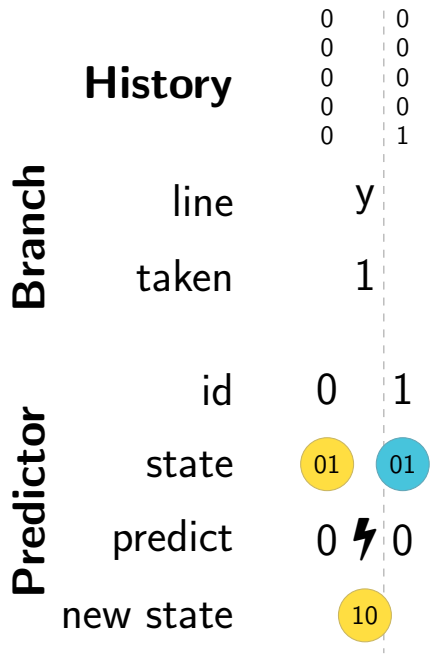


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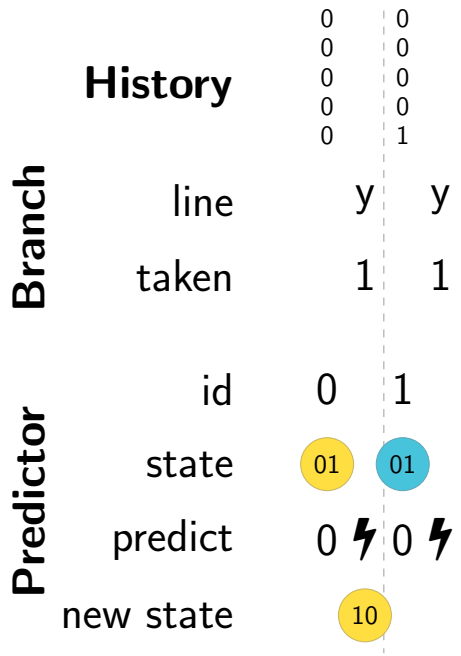


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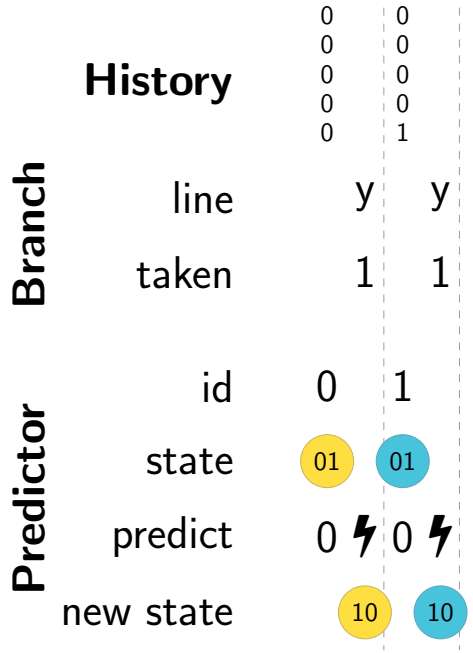


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        addi s1, s1, -1
branch y → bnez s1, yloop
        addi s0, s0, -1
branch x → bnez s0, xloop
```
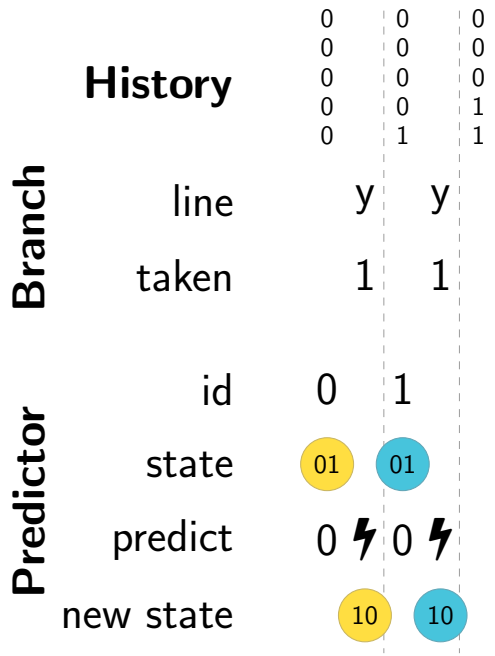

Adaptive Predictor: Example

5 bit of history (init: 00000), 32 Predictors

2-bit predictors (init: 01)

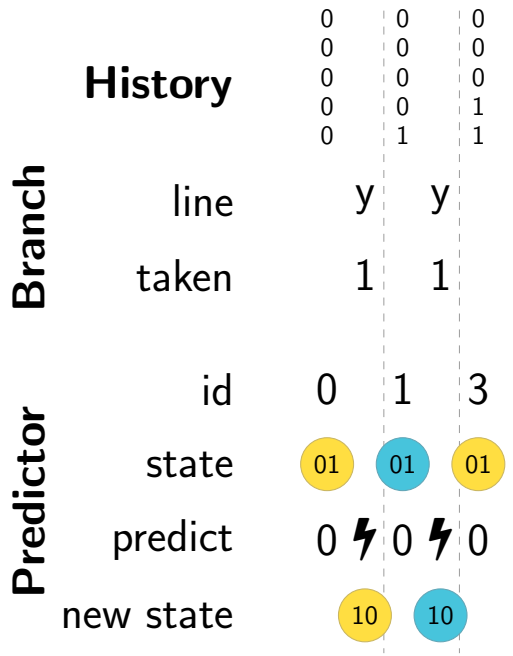



```
        li s0, 1024
xloop:  li s1, 4
yloop:  mv a0, s0
        mv a1, s1
        jal ra, do_something
        addi s1, s1, -1
branch y →bnez s1, yloop
        addi s0, s0, -1
branch x →bnez s0, xloop
```

Adaptive Predictor: Example

5 bit of history (init: 00000), 32 Predictors

2-bit predictors (init: 01)

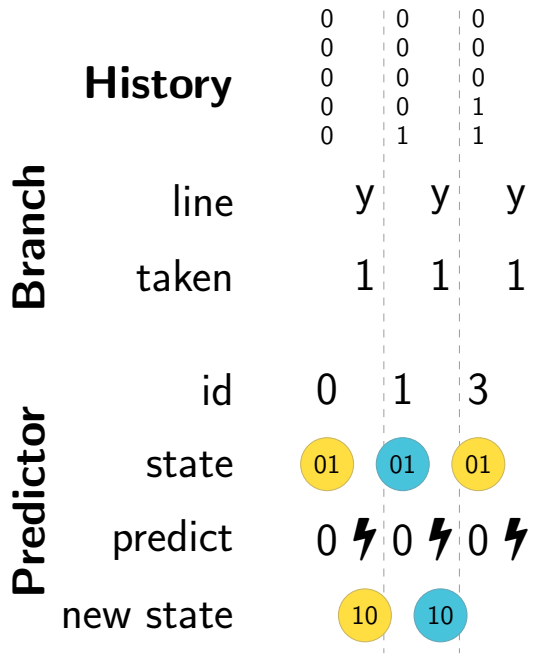



```
        li s0, 1024
xloop:  li s1, 4
yloop:  mv a0, s0
        mv a1, s1
        jal ra, do_something
        addi s1, s1, -1
branch y →bnez s1, yloop
        addi s0, s0, -1
branch x →bnez s0, xloop
```

Adaptive Predictor: Example

5 bit of history (init: 00000), 32 Predictors

2-bit predictors (init: 01)

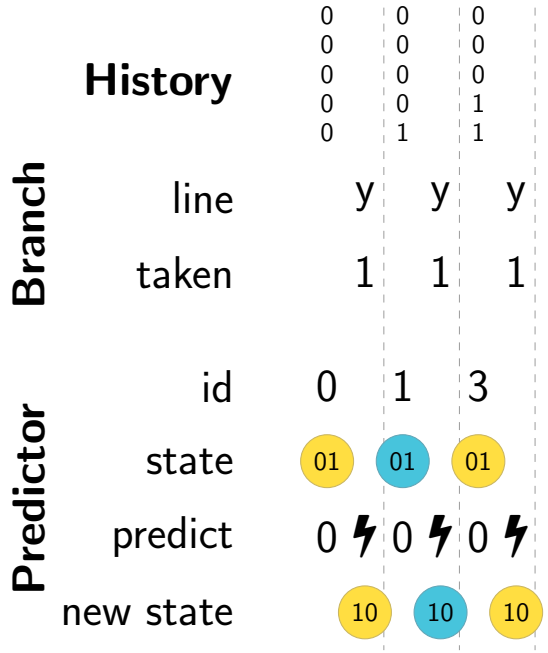



```
        li s0, 1024
xloop:  li s1, 4
yloop:  mv a0, s0
        mv a1, s1
        jal ra, do_something
        addi s1, s1, -1
branch y →bnez s1, yloop
        addi s0, s0, -1
branch x →bnez s0, xloop
```

Adaptive Predictor: Example

5 bit of history (init: 00000), 32 Predictors

2-bit predictors (init: 01)

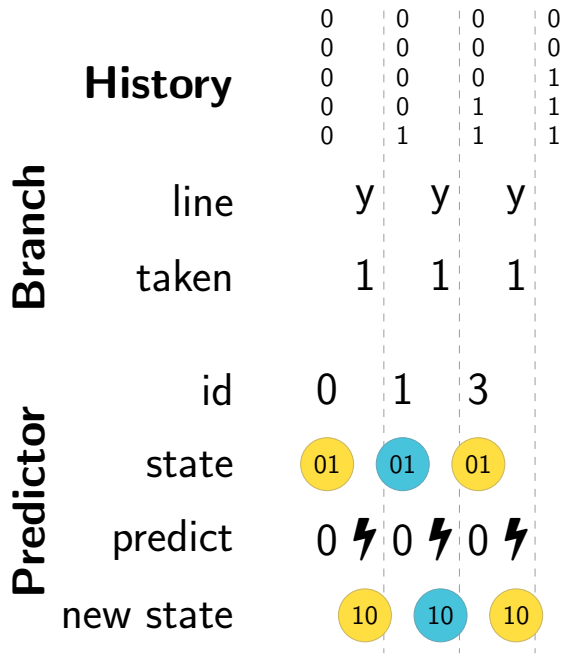



```
        li s0, 1024
xloop:  li s1, 4
yloop:  mv a0, s0
        mv a1, s1
        jal ra, do_something
        addi s1, s1, -1
branch y →bnez s1, yloop
        addi s0, s0, -1
branch x →bnez s0, xloop
```

Adaptive Predictor: Example

5 bit of history (init: 00000), 32 Predictors

2-bit predictors (init: 01)

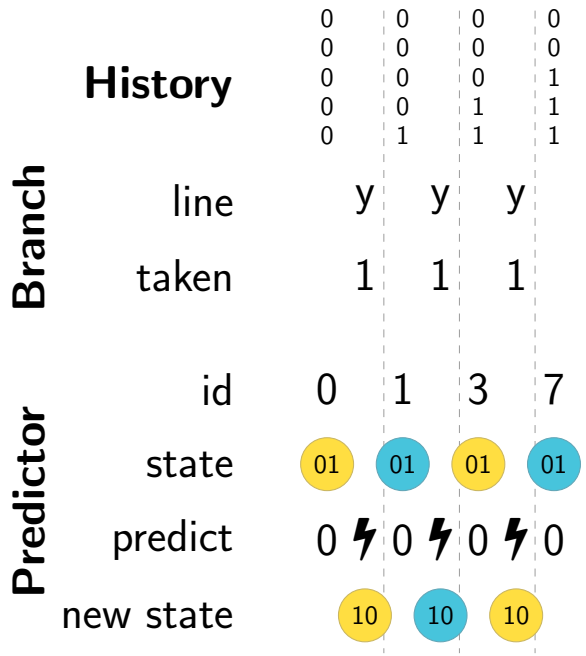



```
        li s0, 1024
xloop:  li s1, 4
yloop:  mv a0, s0
        mv a1, s1
        jal ra, do_something
        addi s1, s1, -1
branch y →bnez s1, yloop
        addi s0, s0, -1
branch x →bnez s0, xloop
```

Adaptive Predictor: Example

5 bit of history (init: 00000), 32 Predictors

2-bit predictors (init: 01)

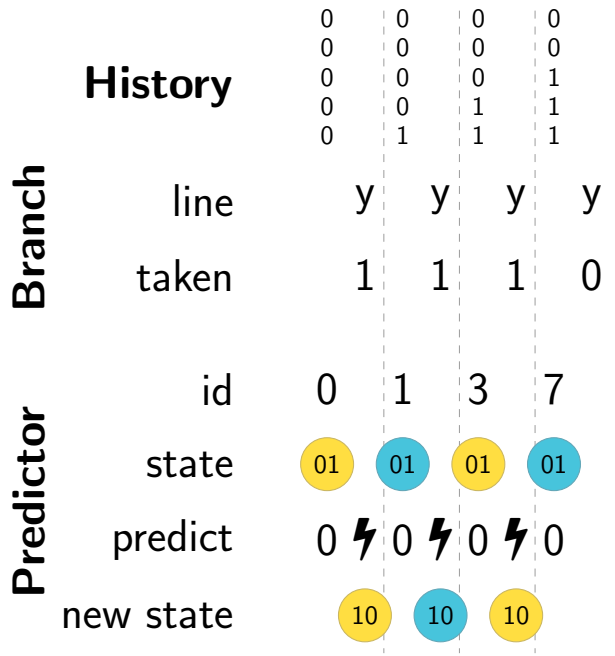



```
        li s0, 1024
xloop:  li s1, 4
yloop:  mv a0, s0
        mv a1, s1
        jal ra, do_something
        addi s1, s1, -1
branch y →bnez s1, yloop
        addi s0, s0, -1
branch x →bnez s0, xloop
```

Adaptive Predictor: Example

5 bit of history (init: 00000), 32 Predictors

2-bit predictors (init: 01)

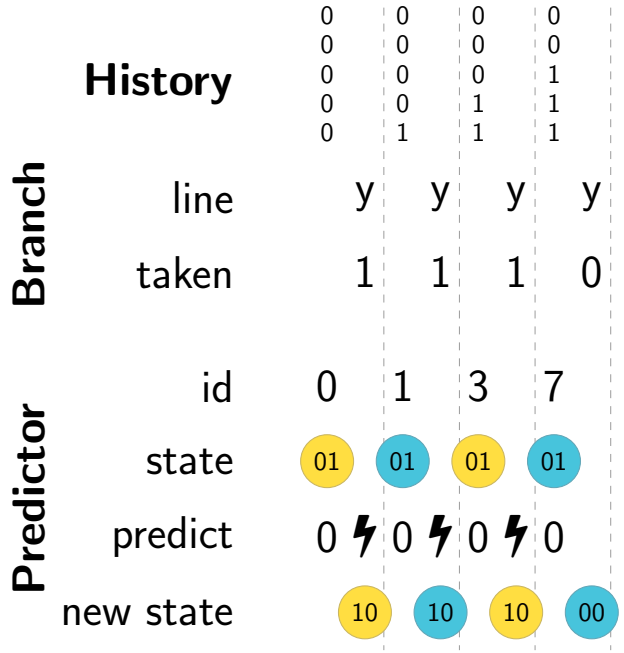



```
        li s0, 1024
xloop:  li s1, 4
yloop:  mv a0, s0
        mv a1, s1
        jal ra, do_something
        addi s1, s1, -1
branch y →bnez s1, yloop
        addi s0, s0, -1
branch x →bnez s0, xloop
```

Adaptive Predictor: Example

5 bit of history (init: 00000), 32 Predictors

2-bit predictors (init: 01)

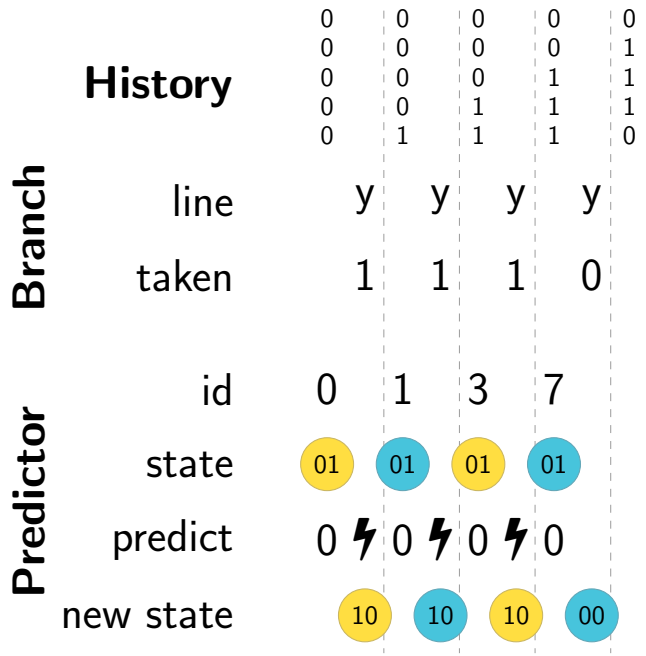



```
        li s0, 1024
xloop:  li s1, 4
yloop:  mv a0, s0
        mv a1, s1
        jal ra, do_something
        addi s1, s1, -1
branch y →bnez s1, yloop
        addi s0, s0, -1
branch x →bnez s0, xloop
```

Adaptive Predictor: Example

5 bit of history (init: 00000), 32 Predictors

2-bit predictors (init: 01)

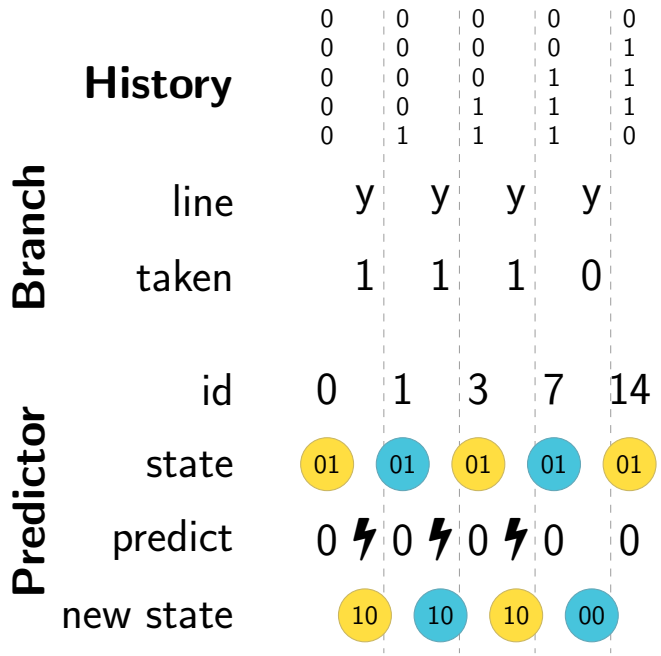



```
        li s0, 1024
xloop:  li s1, 4
yloop:  mv a0, s0
        mv a1, s1
        jal ra, do_something
        addi s1, s1, -1
branch y → bnez s1, yloop
        addi s0, s0, -1
branch x → bnez s0, xloop
```

Adaptive Predictor: Example

5 bit of history (init: 00000), 32 Predictors

2-bit predictors (init: 01)

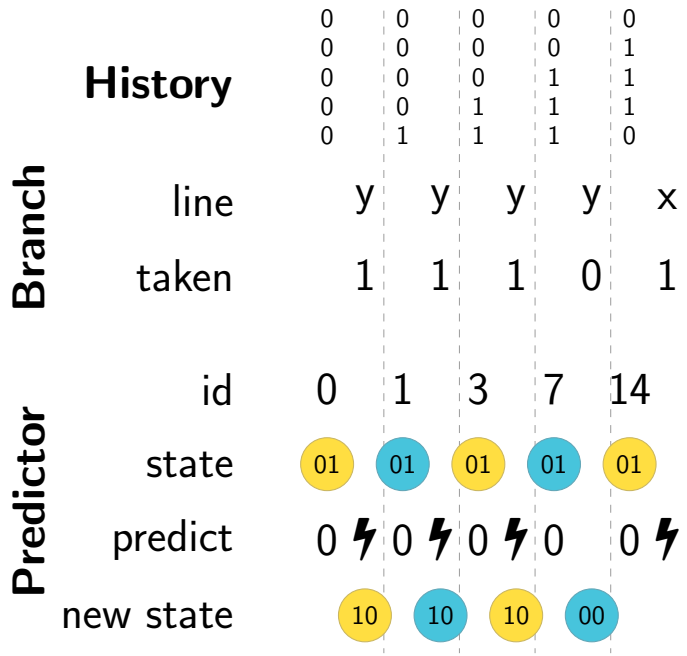



```
        li s0, 1024
xloop:  li s1, 4
yloop:  mv a0, s0
        mv a1, s1
        jal ra, do_something
        addi s1, s1, -1
branch y →bnez s1, yloop
        addi s0, s0, -1
branch x →bnez s0, xloop
```

Adaptive Predictor: Example

5 bit of history (init: 00000), 32 Predictors

2-bit predictors (init: 01)

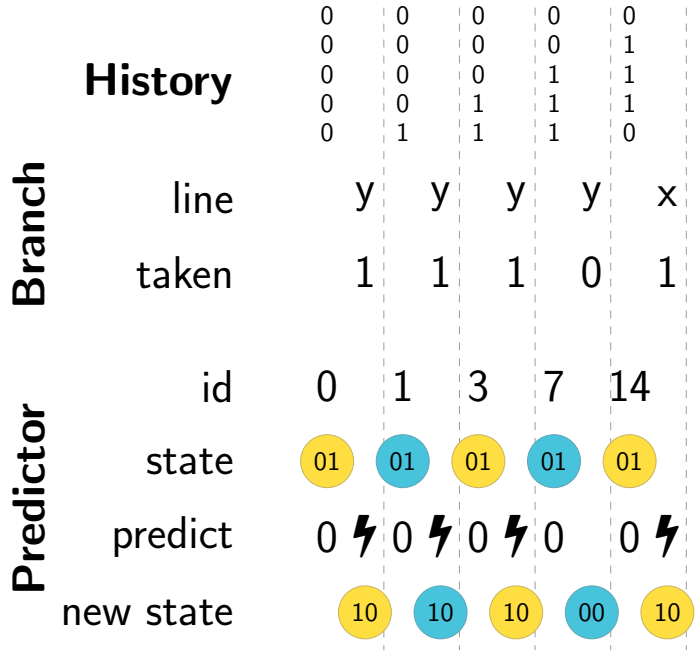



```
        li s0, 1024
xloop:  li s1, 4
yloop:  mv a0, s0
        mv a1, s1
        jal ra, do_something
        addi s1, s1, -1
branch y → bnez s1, yloop
        addi s0, s0, -1
branch x → bnez s0, xloop
```

Adaptive Predictor: Example

5 bit of history (init: 00000), 32 Predictors

2-bit predictors (init: 01)

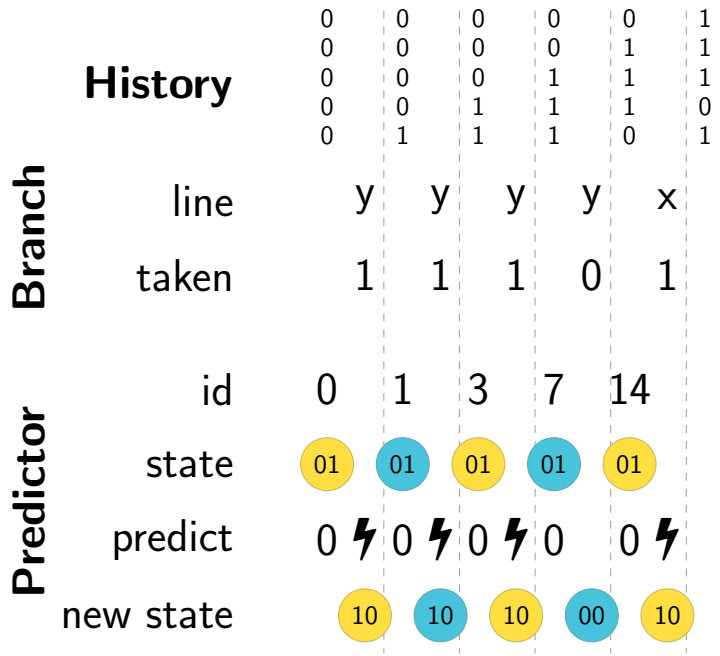



```
        li s0, 1024
xloop:  li s1, 4
yloop:  mv a0, s0
        mv a1, s1
        jal ra, do_something
        addi s1, s1, -1
branch y →bnez s1, yloop
        addi s0, s0, -1
branch x →bnez s0, xloop
```

Adaptive Predictor: Example

5 bit of history (init: 00000), 32 Predictors

2-bit predictors (init: 01)

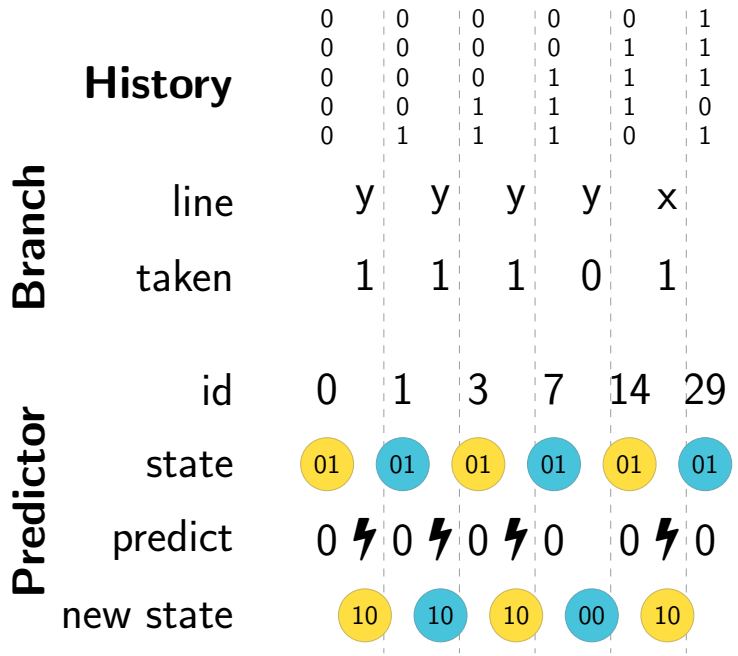



```
        li s0, 1024
xloop:  li s1, 4
yloop:  mv a0, s0
        mv a1, s1
        jal ra, do_something
        addi s1, s1, -1
branch y →bnez s1, yloop
        addi s0, s0, -1
branch x →bnez s0, xloop
```

Adaptive Predictor: Example

5 bit of history (init: 00000), 32 Predictors

2-bit predictors (init: 01)

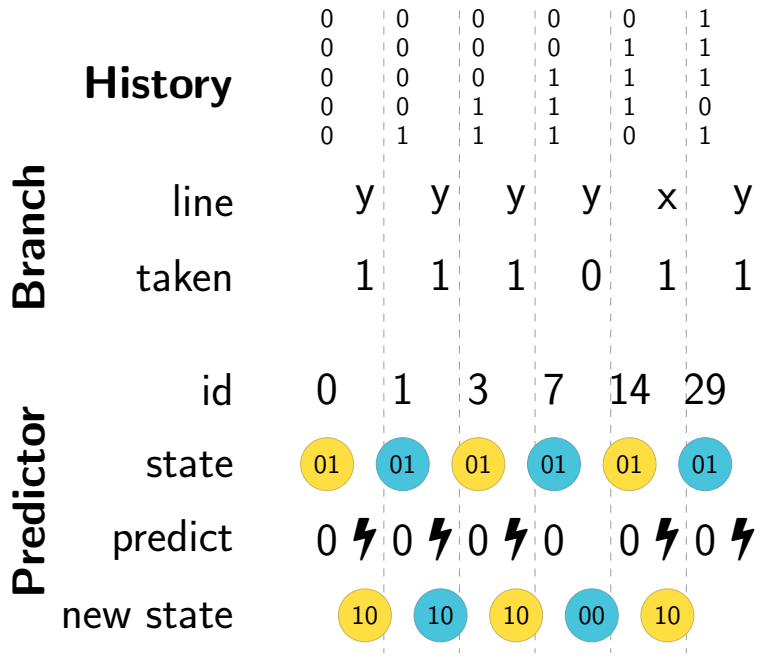



```
        li s0, 1024
xloop:  li s1, 4
yloop:  mv a0, s0
        mv a1, s1
        jal ra, do_something
        addi s1, s1, -1
branch y →bnez s1, yloop
        addi s0, s0, -1
branch x →bnez s0, xloop
```

Adaptive Predictor: Example

5 bit of history (init: 00000), 32 Predictors

2-bit predictors (init: 01)

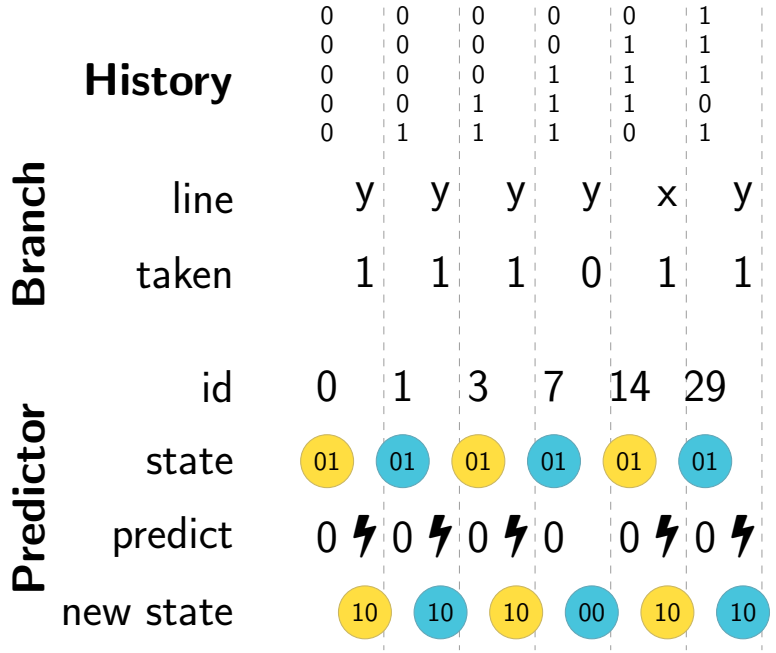



```
        li s0, 1024
xloop:  li s1, 4
yloop:  mv a0, s0
        mv a1, s1
        jal ra, do_something
        addi s1, s1, -1
branch y →bnez s1, yloop
        addi s0, s0, -1
branch x →bnez s0, xloop
```

Adaptive Predictor: Example

5 bit of history (init: 00000), 32 Predictors

2-bit predictors (init: 01)

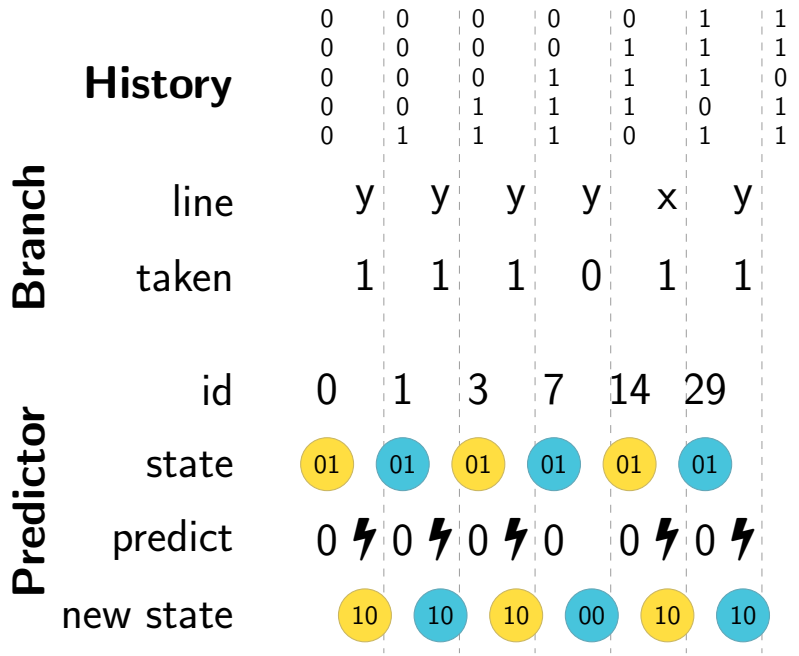



```
        li s0, 1024
xloop:  li s1, 4
yloop:  mv a0, s0
        mv a1, s1
        jal ra, do_something
        addi s1, s1, -1
branch y →bnez s1, yloop
        addi s0, s0, -1
branch x →bnez s0, xloop
```

Adaptive Predictor: Example

5 bit of history (init: 00000), 32 Predictors

2-bit predictors (init: 01)

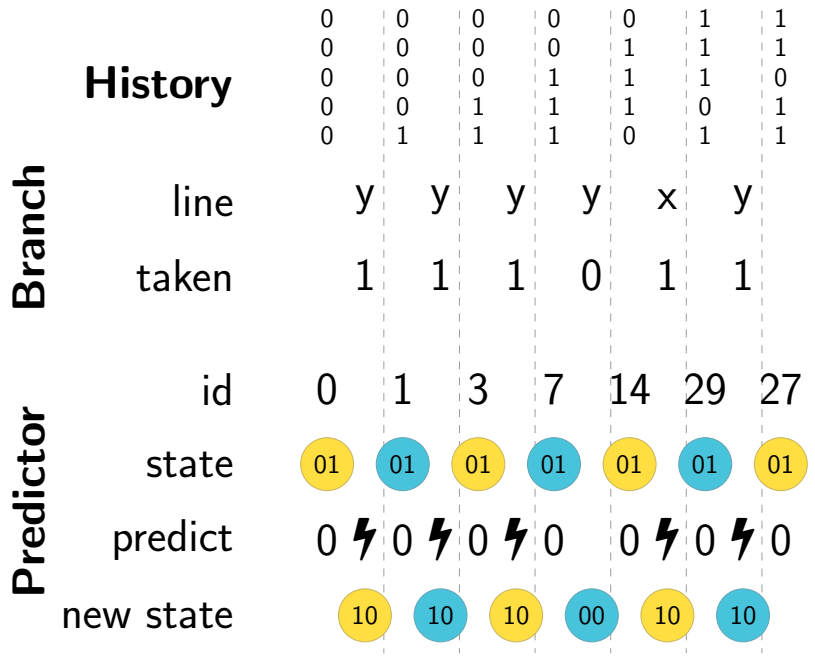



```
        li s0, 1024
xloop:  li s1, 4
yloop:  mv a0, s0
        mv a1, s1
        jal ra, do_something
        addi s1, s1, -1
branch y →bnez s1, yloop
        addi s0, s0, -1
branch x →bnez s0, xloop
```

Adaptive Predictor: Example

5 bit of history (init: 00000), 32 Predictors

2-bit predictors (init: 01)

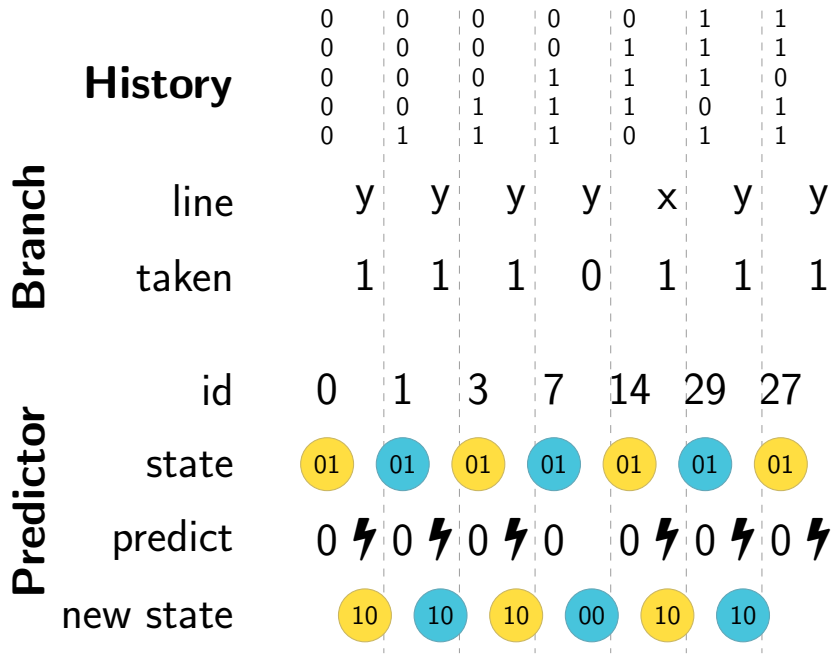



```
        li s0, 1024
xloop:  li s1, 4
yloop:  mv a0, s0
        mv a1, s1
        jal ra, do_something
        addi s1, s1, -1
branch y →bnez s1, yloop
        addi s0, s0, -1
branch x →bnez s0, xloop
```

Adaptive Predictor: Example

5 bit of history (init: 00000), 32 Predictors

2-bit predictors (init: 01)

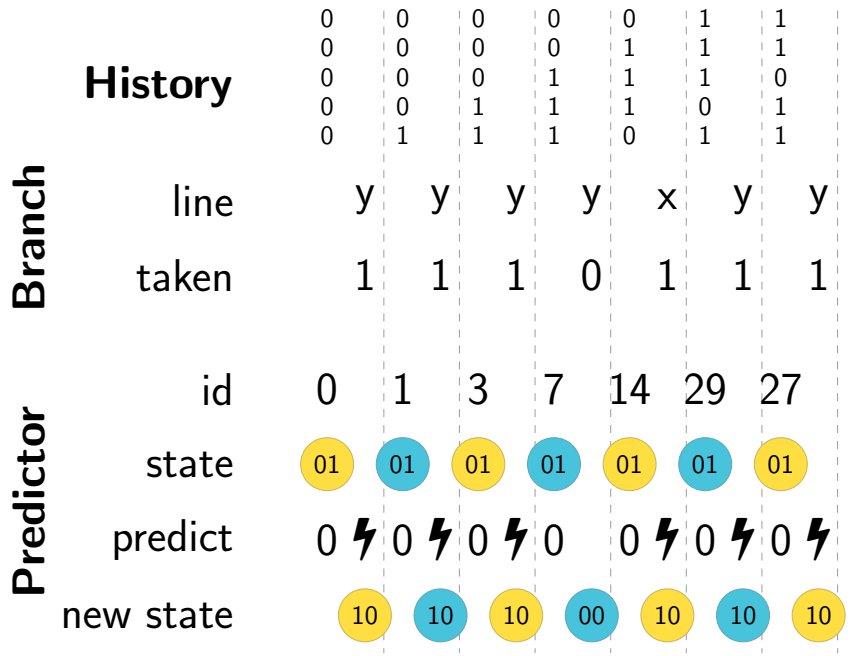



```
        li s0, 1024
xloop:  li s1, 4
yloop:  mv a0, s0
        mv a1, s1
        jal ra, do_something
        addi s1, s1, -1
branch y →bnez s1, yloop
        addi s0, s0, -1
branch x →bnez s0, xloop
```

Adaptive Predictor: Example

5 bit of history (init: 00000), 32 Predictors

2-bit predictors (init: 01)

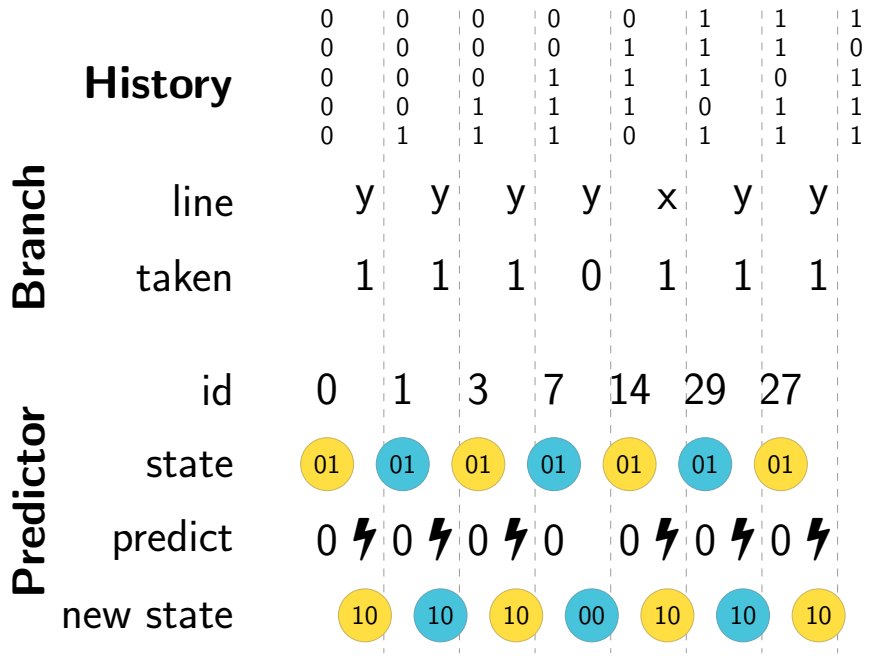



```
        li s0, 1024
xloop:  li s1, 4
yloop:  mv a0, s0
        mv a1, s1
        jal ra, do_something
        addi s1, s1, -1
branch y →bnez s1, yloop
        addi s0, s0, -1
branch x →bnez s0, xloop
```

Adaptive Predictor: Example

5 bit of history (init: 00000), 32 Predictors

2-bit predictors (init: 01)

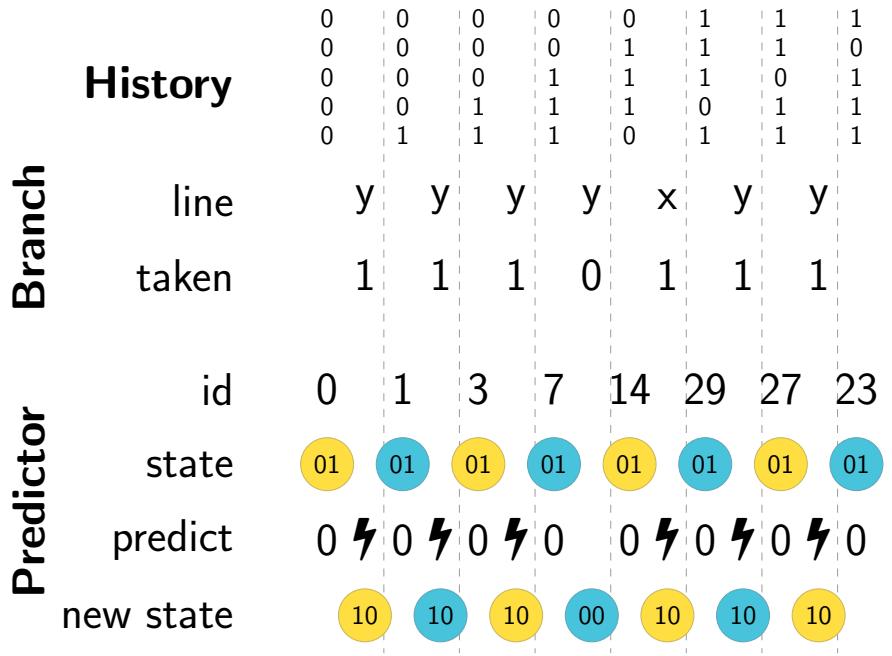



```
        li s0, 1024
xloop:  li s1, 4
yloop:  mv a0, s0
        mv a1, s1
        jal ra, do_something
        addi s1, s1, -1
branch y →bnez s1, yloop
        addi s0, s0, -1
branch x →bnez s0, xloop
```

Adaptive Predictor: Example

5 bit of history (init: 00000), 32 Predictors

2-bit predictors (init: 01)

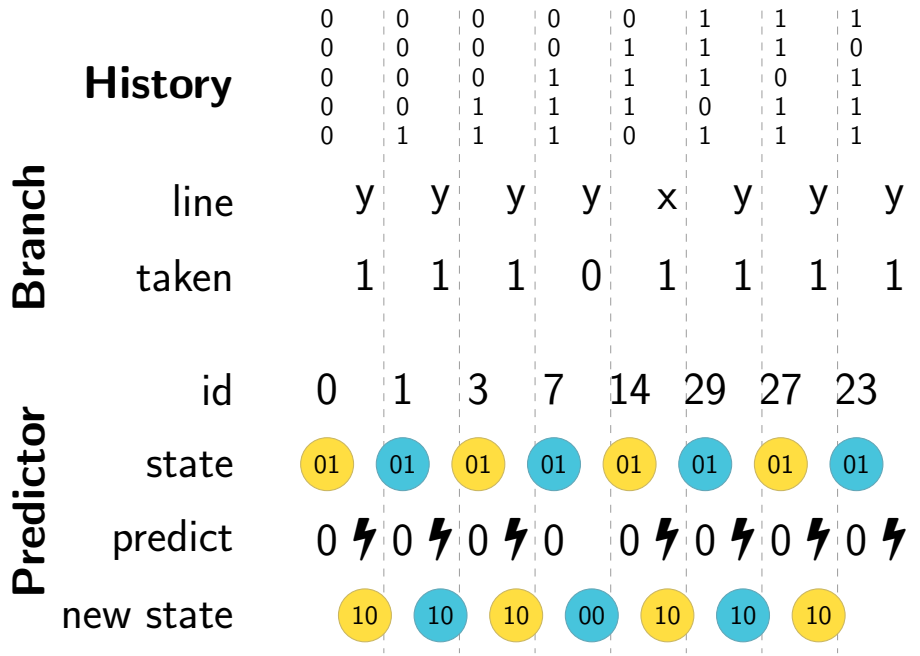



```
        li s0, 1024
xloop:  li s1, 4
yloop:  mv a0, s0
        mv a1, s1
        jal ra, do_something
        addi s1, s1, -1
branch y →bnez s1, yloop
        addi s0, s0, -1
branch x →bnez s0, xloop
```

Adaptive Predictor: Example

5 bit of history (init: 00000), 32 Predictors

2-bit predictors (init: 01)

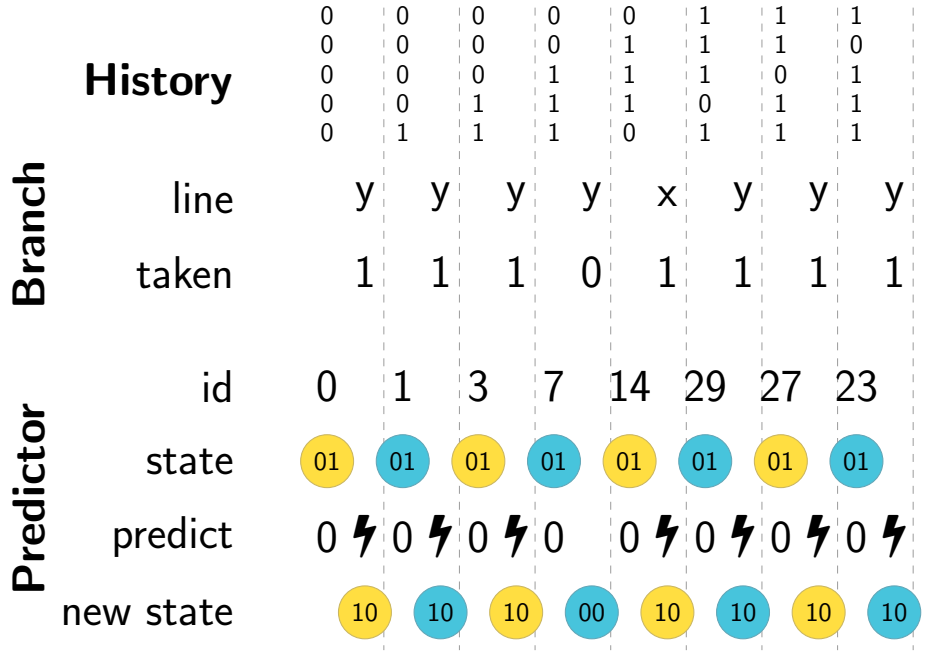



```
        li s0, 1024
xloop:  li s1, 4
yloop:  mv a0, s0
        mv a1, s1
        jal ra, do_something
        addi s1, s1, -1
branch y →bnez s1, yloop
        addi s0, s0, -1
branch x →bnez s0, xloop
```

Adaptive Predictor: Example

5 bit of history (init: 00000), 32 Predictors

2-bit predictors (init: 01)

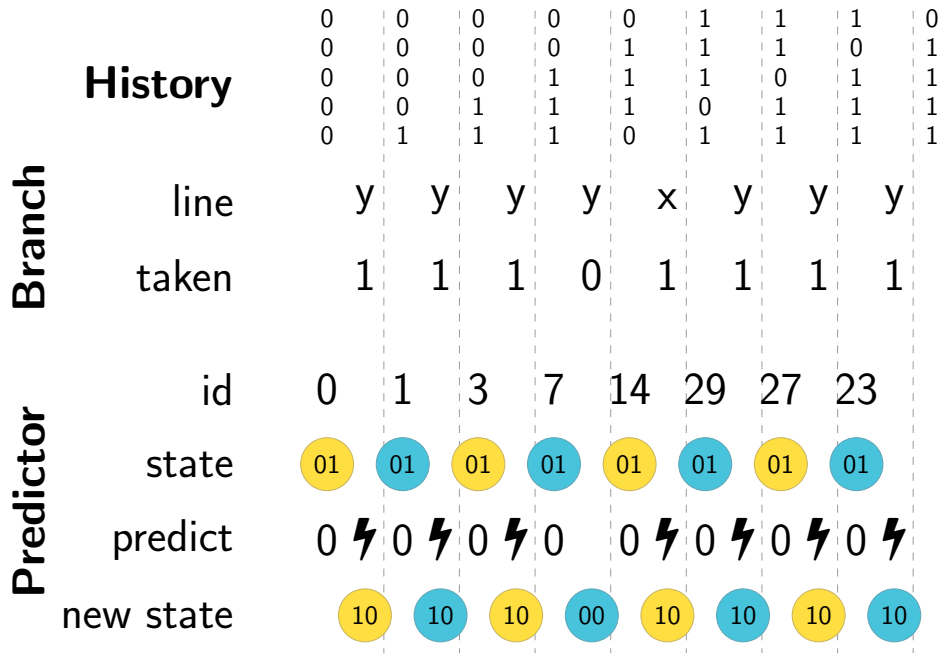



```
        li s0, 1024
xloop:  li s1, 4
yloop:  mv a0, s0
        mv a1, s1
        jal ra, do_something
        addi s1, s1, -1
branch y →bnez s1, yloop
        addi s0, s0, -1
branch x →bnez s0, xloop
```

Adaptive Predictor: Example

5 bit of history (init: 00000), 32 Predictors

2-bit predictors (init: 01)

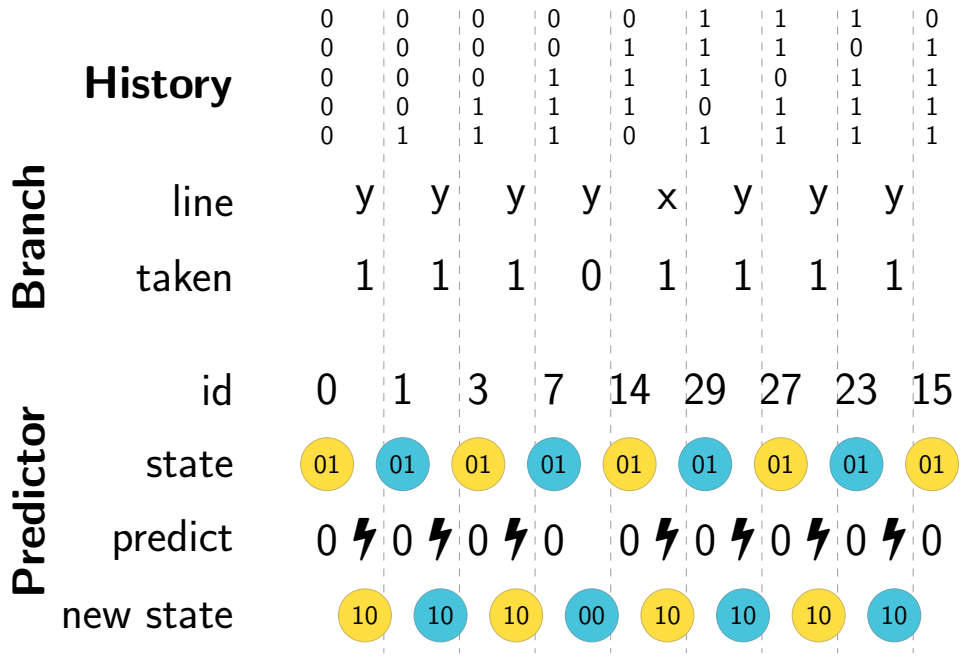



```
        li s0, 1024
xloop:  li s1, 4
yloop:  mv a0, s0
        mv a1, s1
        jal ra, do_something
        addi s1, s1, -1
branch y →bnez s1, yloop
        addi s0, s0, -1
branch x →bnez s0, xloop
```

Adaptive Predictor: Example

5 bit of history (init: 00000), 32 Predictors

2-bit predictors (init: 01)

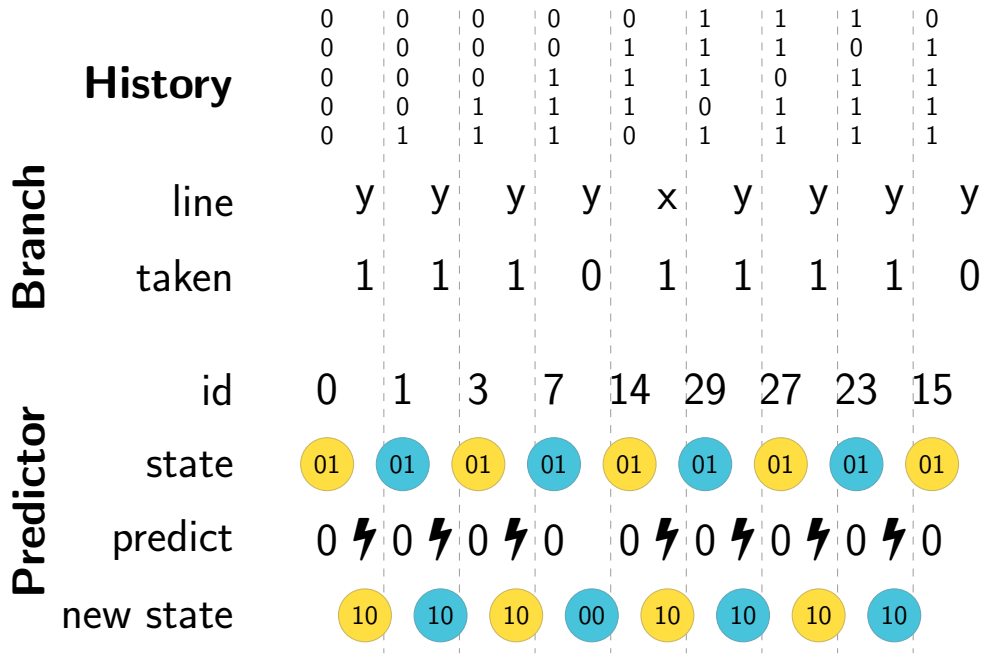



```
        li s0, 1024
xloop:  li s1, 4
yloop:  mv a0, s0
        mv a1, s1
        jal ra, do_something
        addi s1, s1, -1
branch y →bnez s1, yloop
        addi s0, s0, -1
branch x →bnez s0, xloop
```

Adaptive Predictor: Example

5 bit of history (init: 00000), 32 Predictors

2-bit predictors (init: 01)

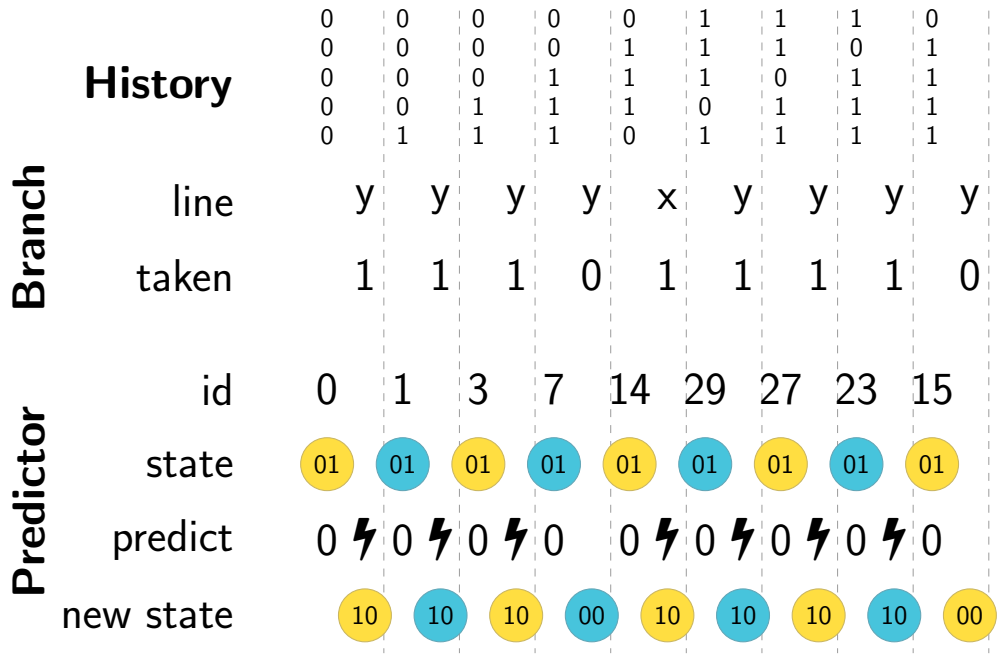



```
        li s0, 1024
xloop:  li s1, 4
yloop:  mv a0, s0
        mv a1, s1
        jal ra, do_something
        addi s1, s1, -1
branch y →bnez s1, yloop
        addi s0, s0, -1
branch x →bnez s0, xloop
```

Adaptive Predictor: Example

5 bit of history (init: 00000), 32 Predictors

2-bit predictors (init: 01)

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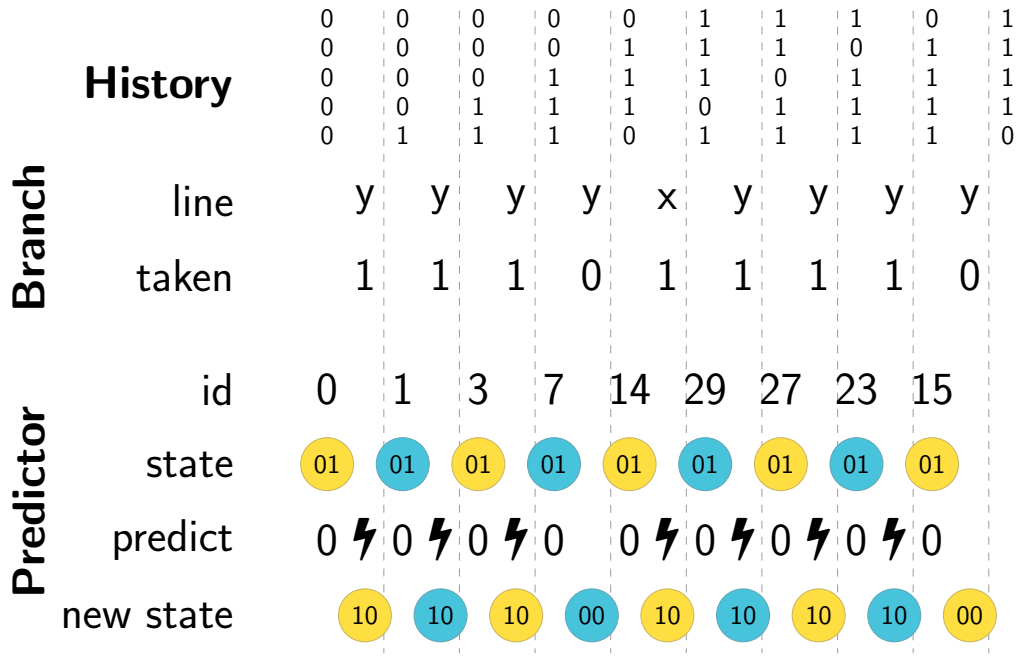


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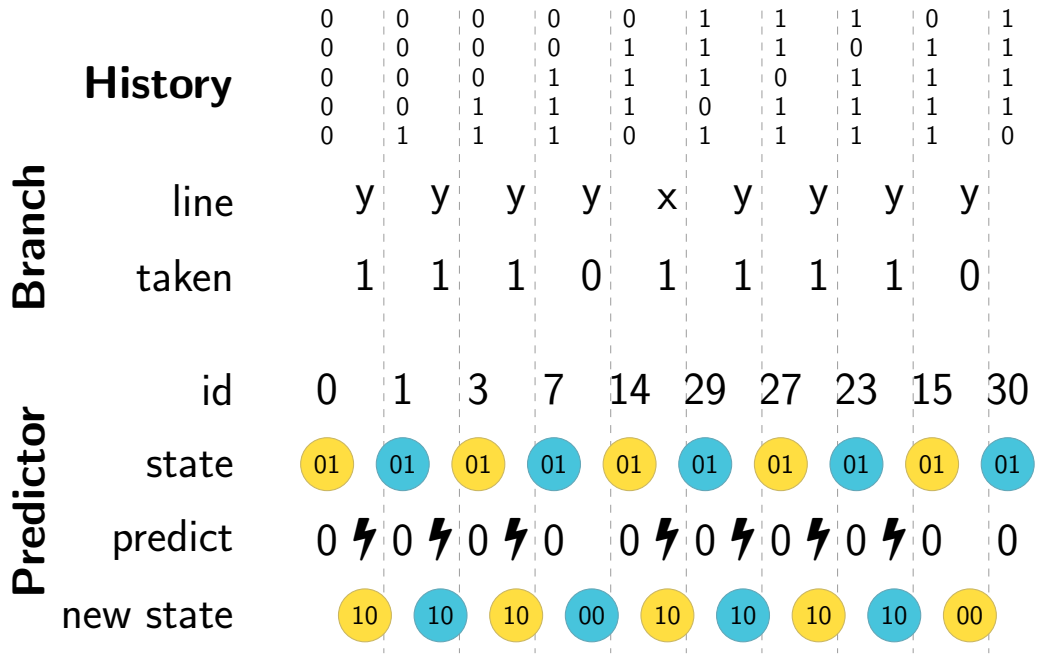


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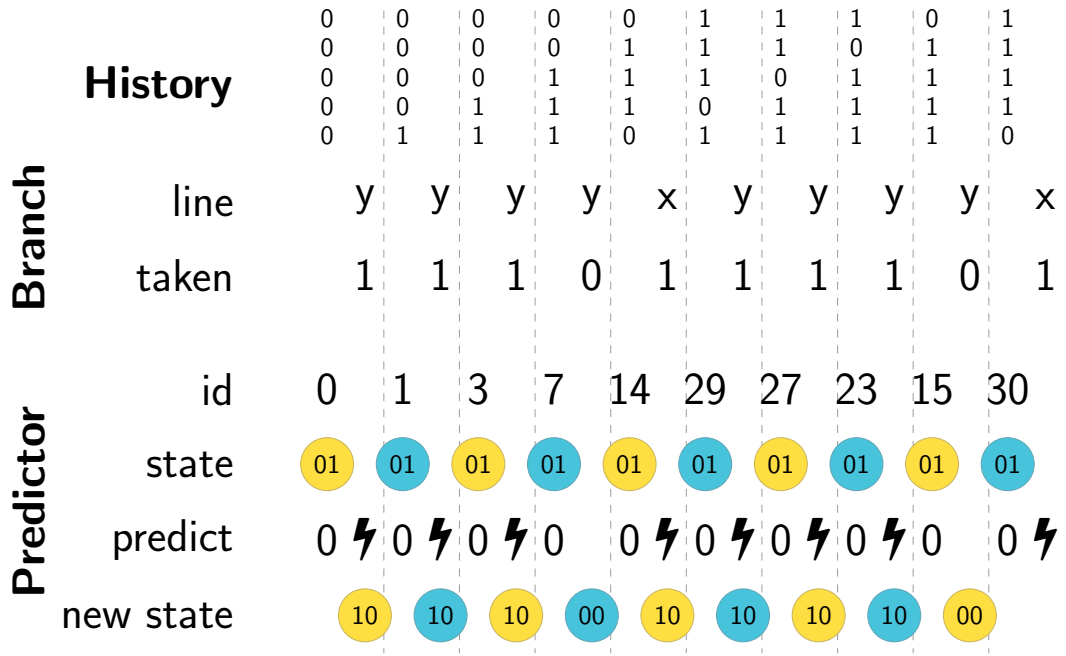


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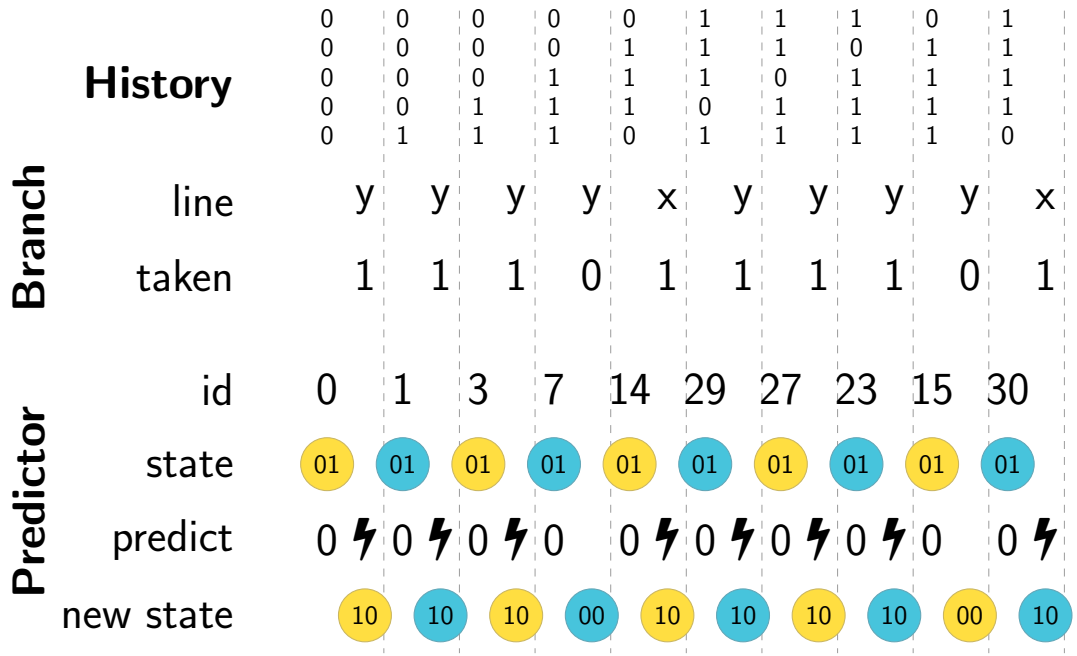


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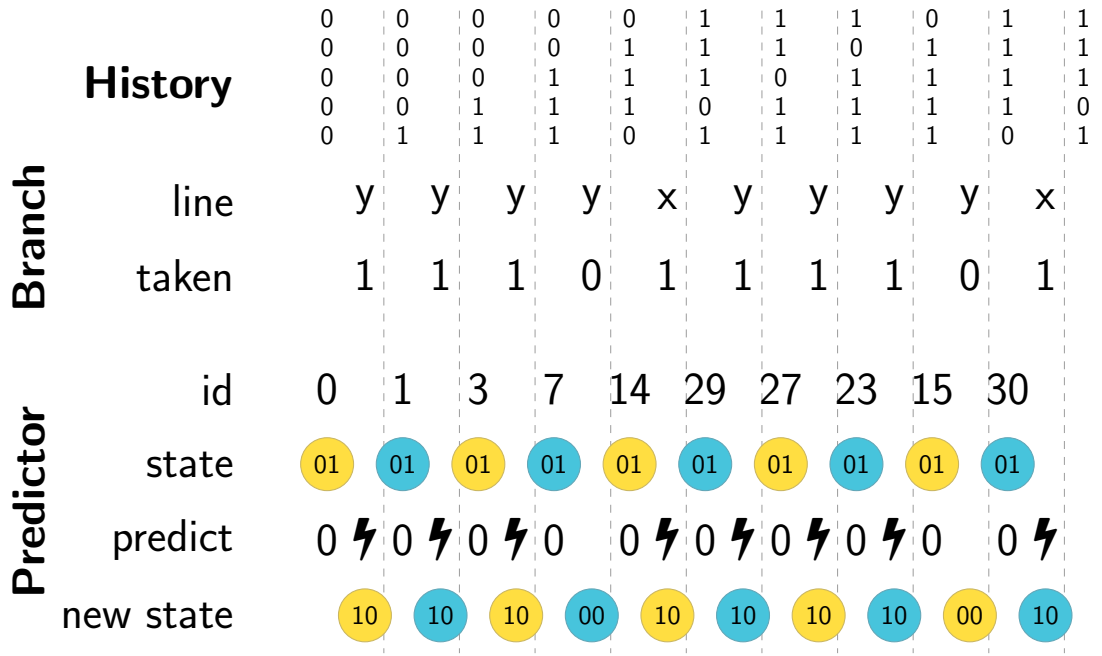


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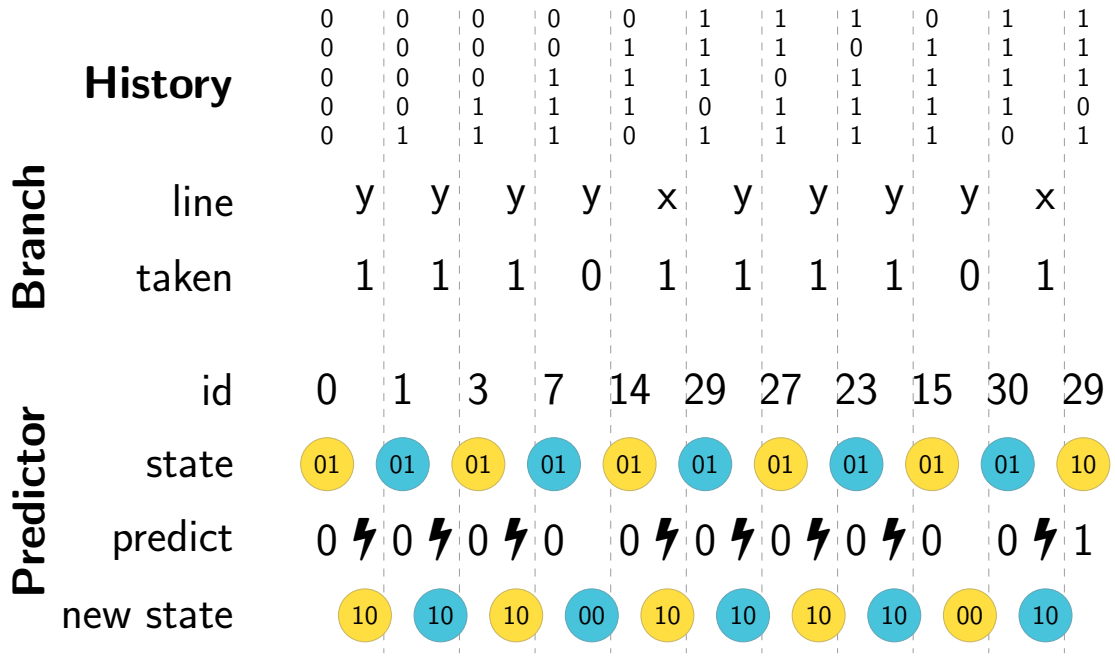


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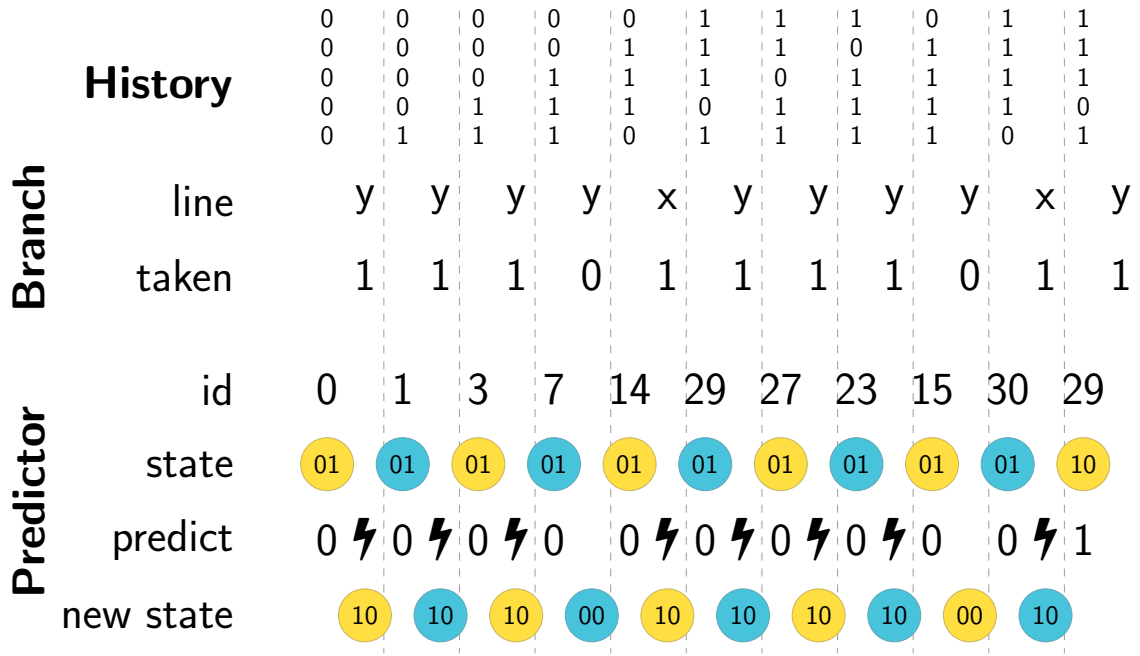


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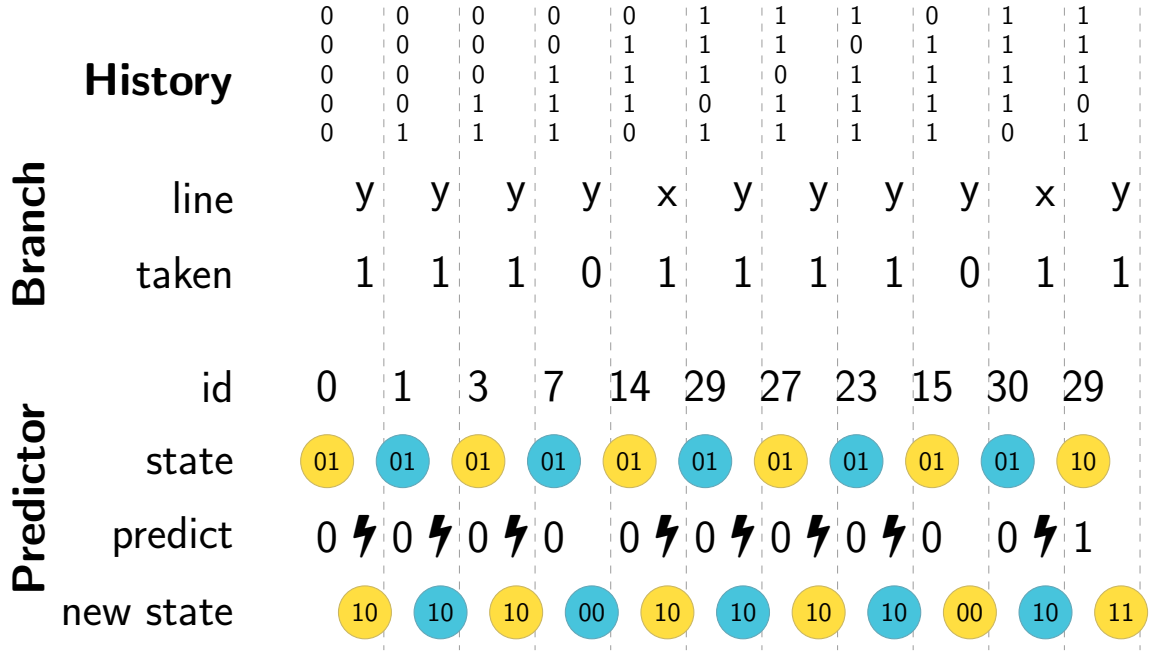


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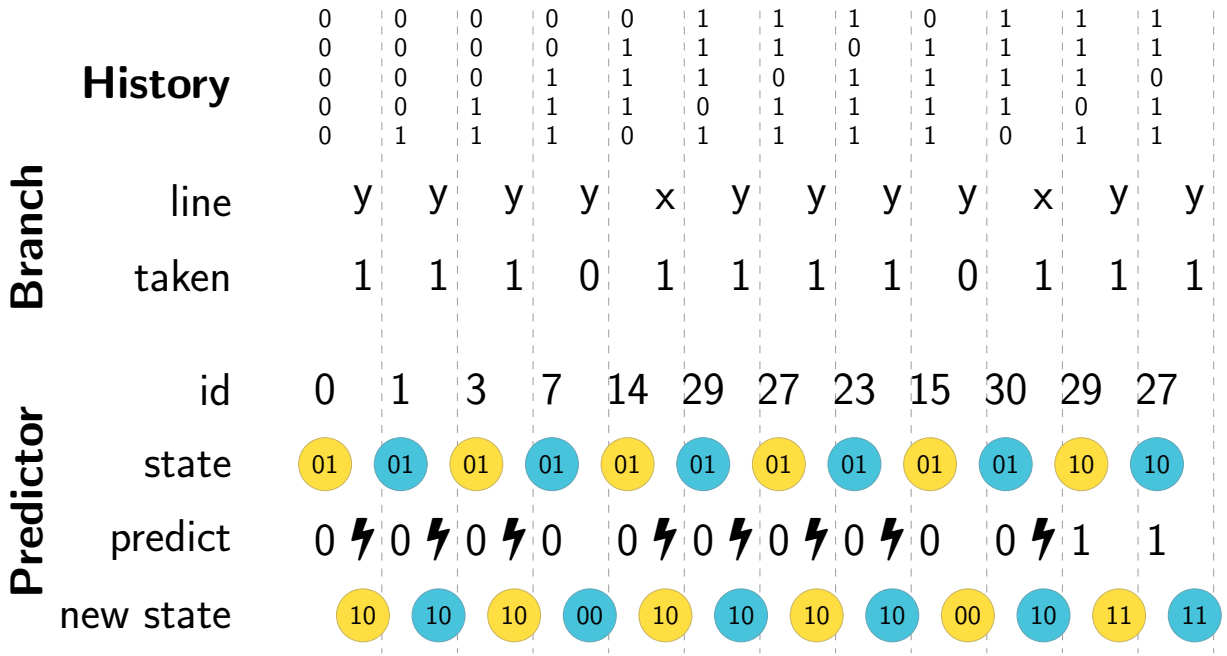

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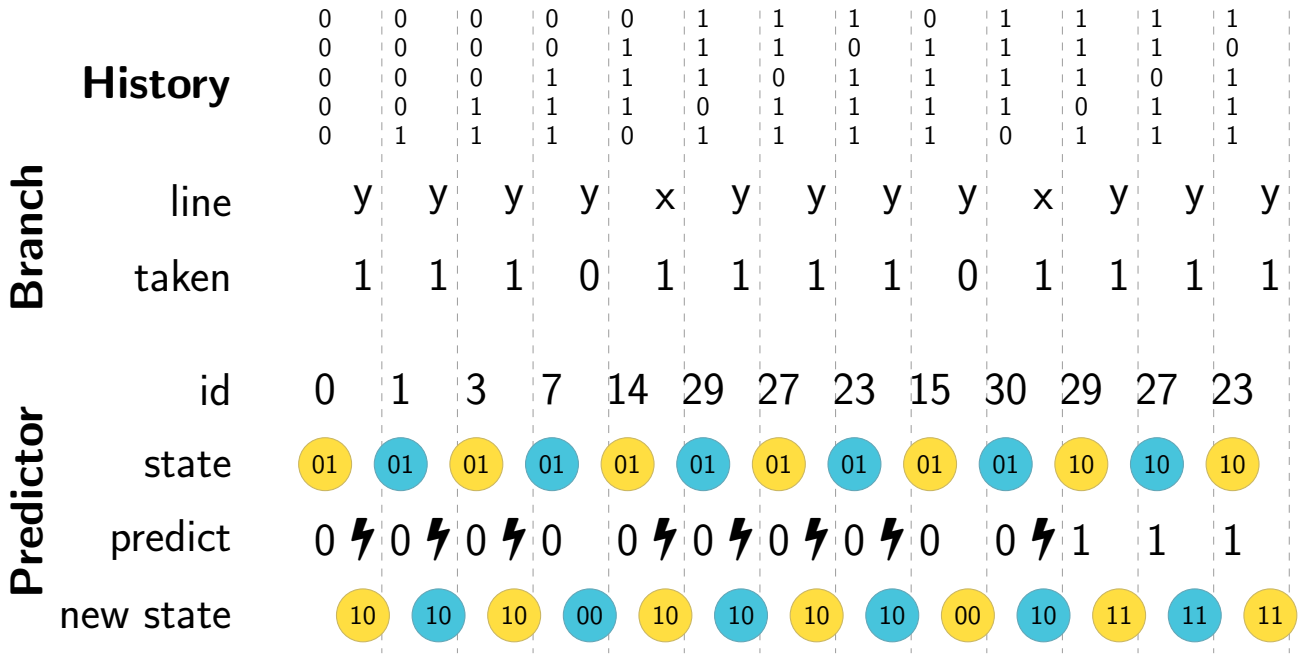

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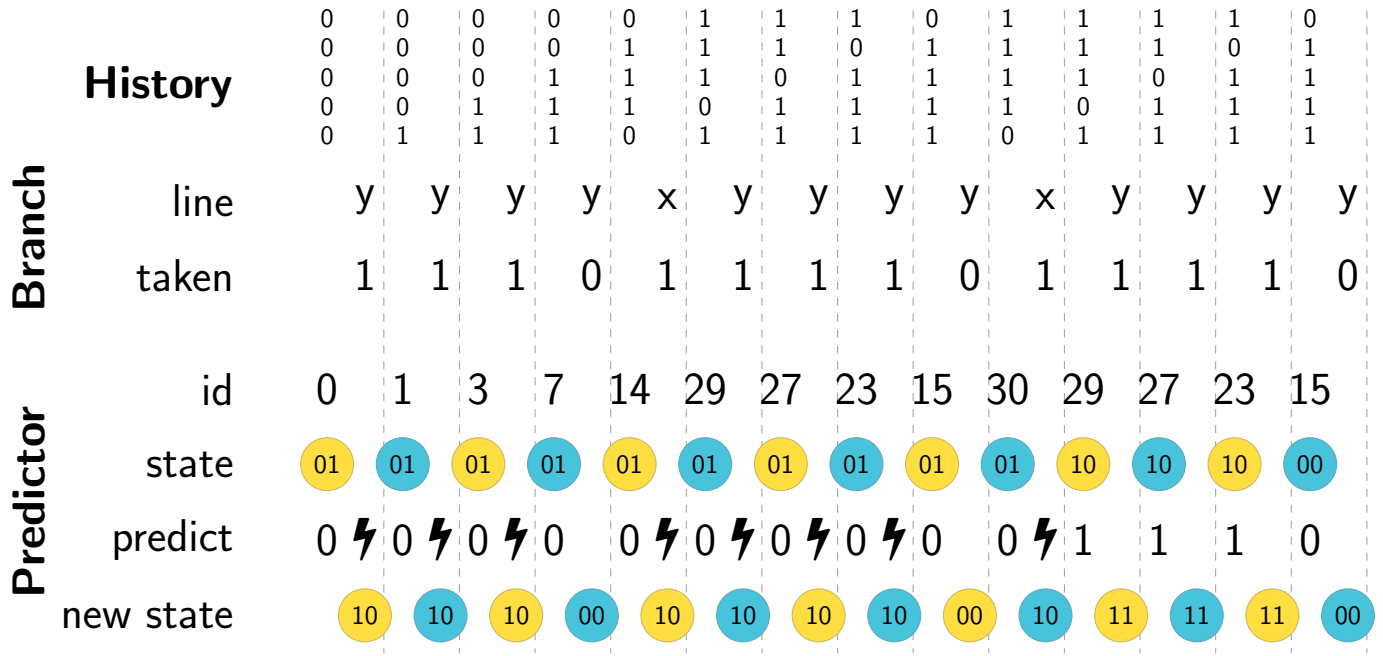

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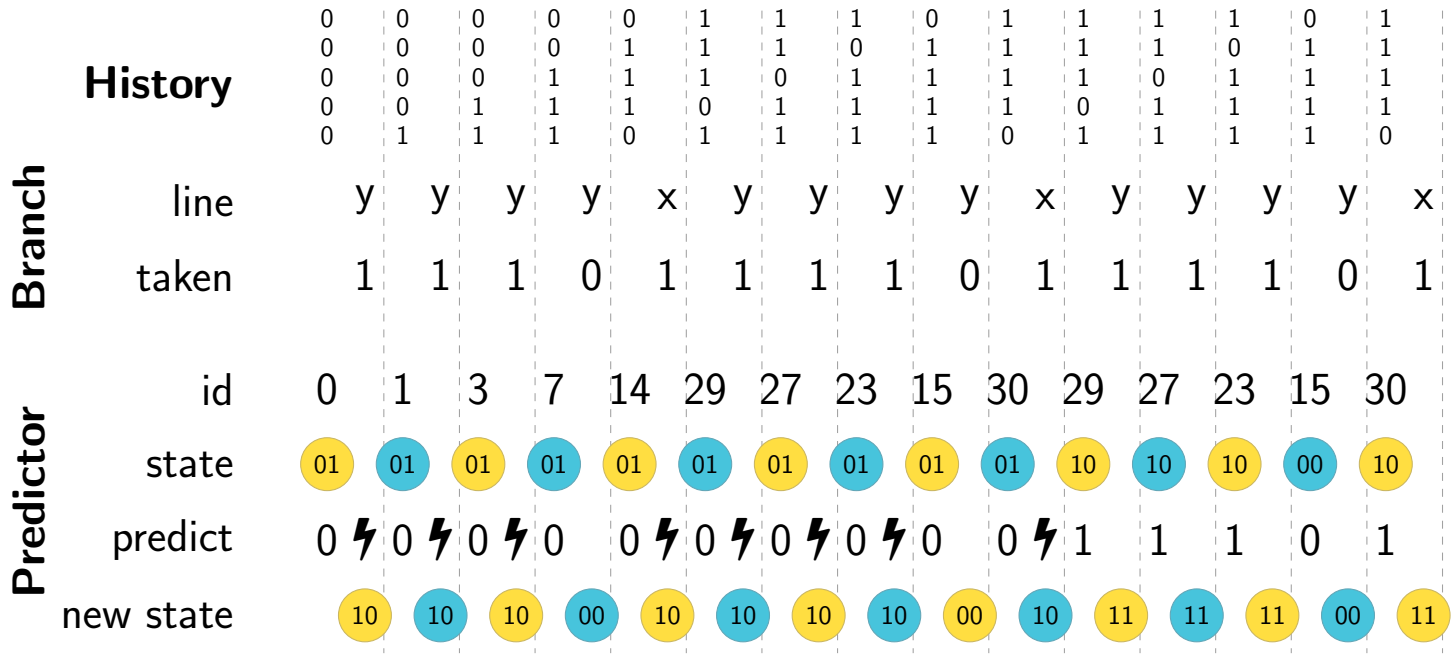

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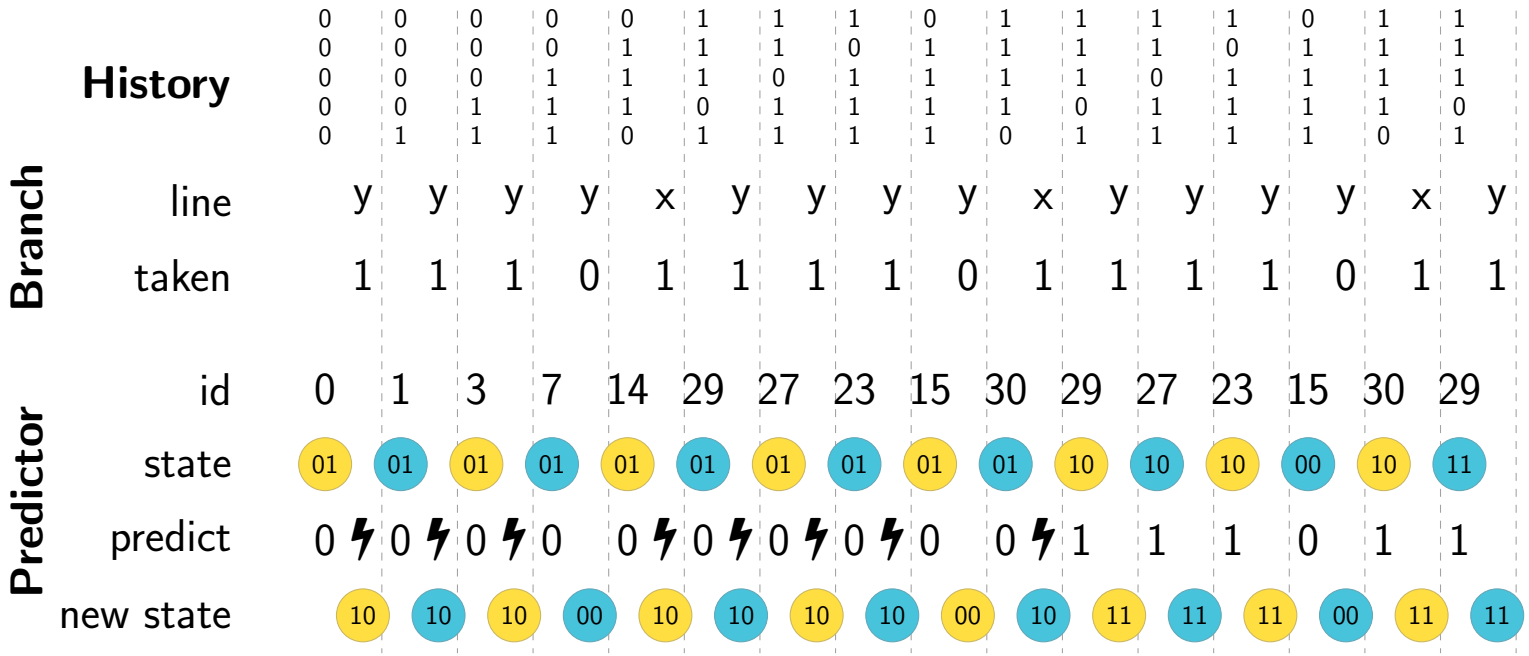

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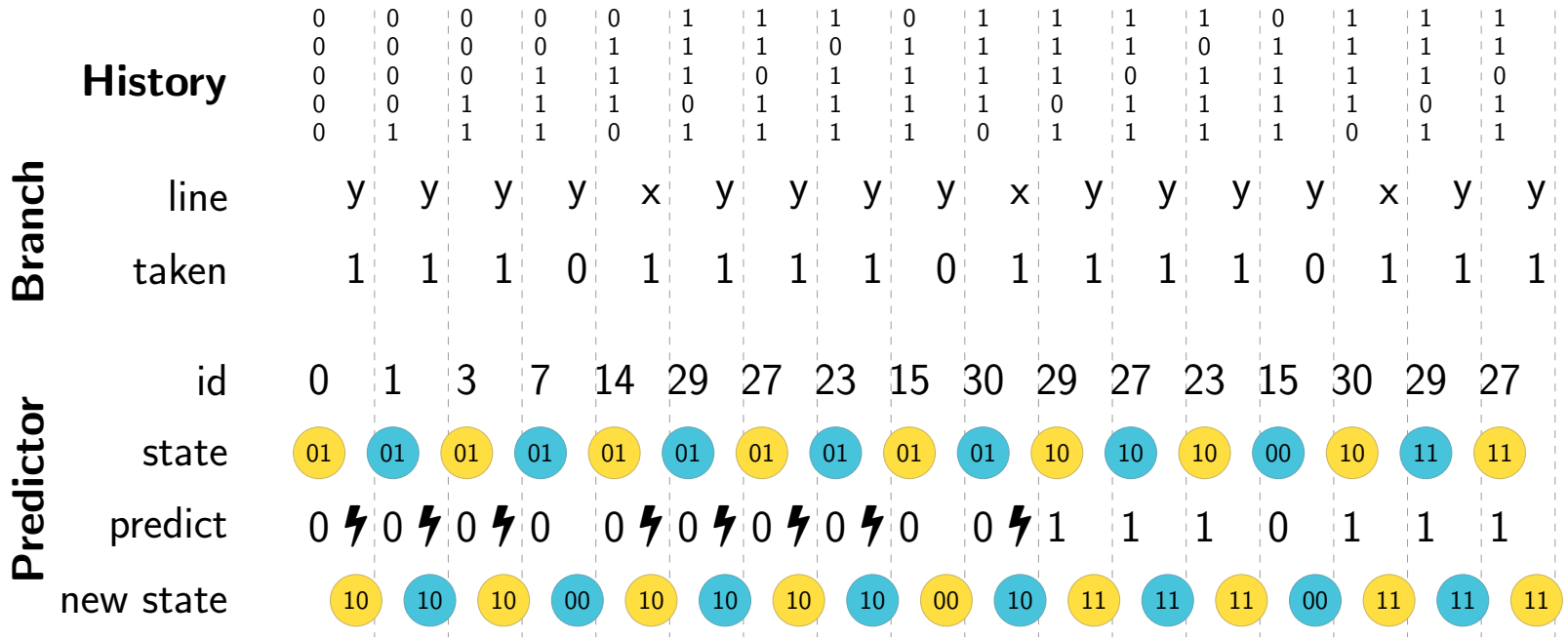

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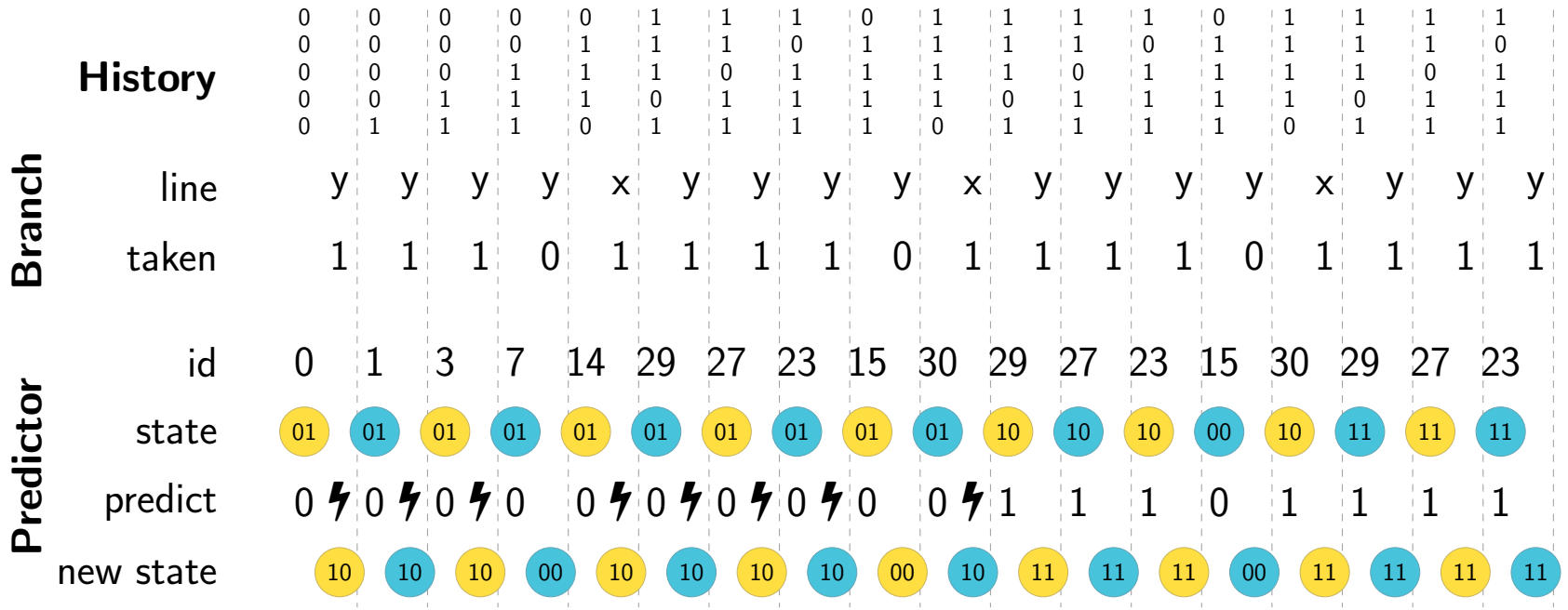

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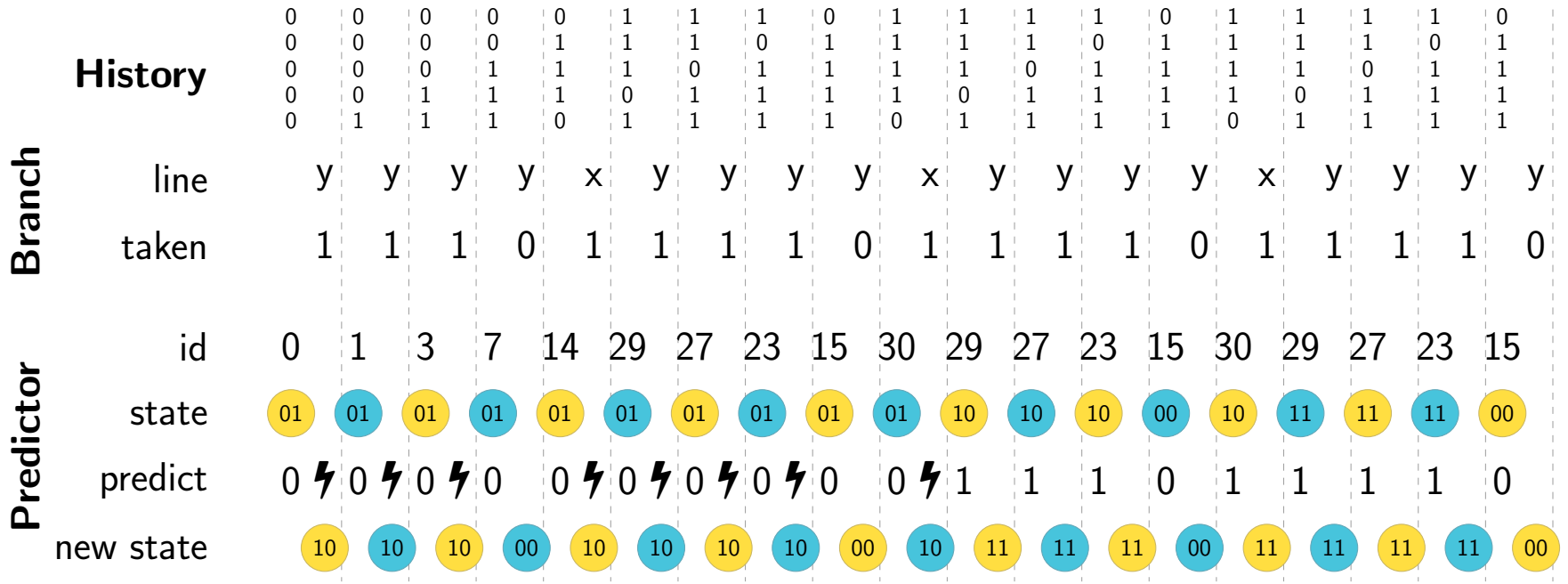

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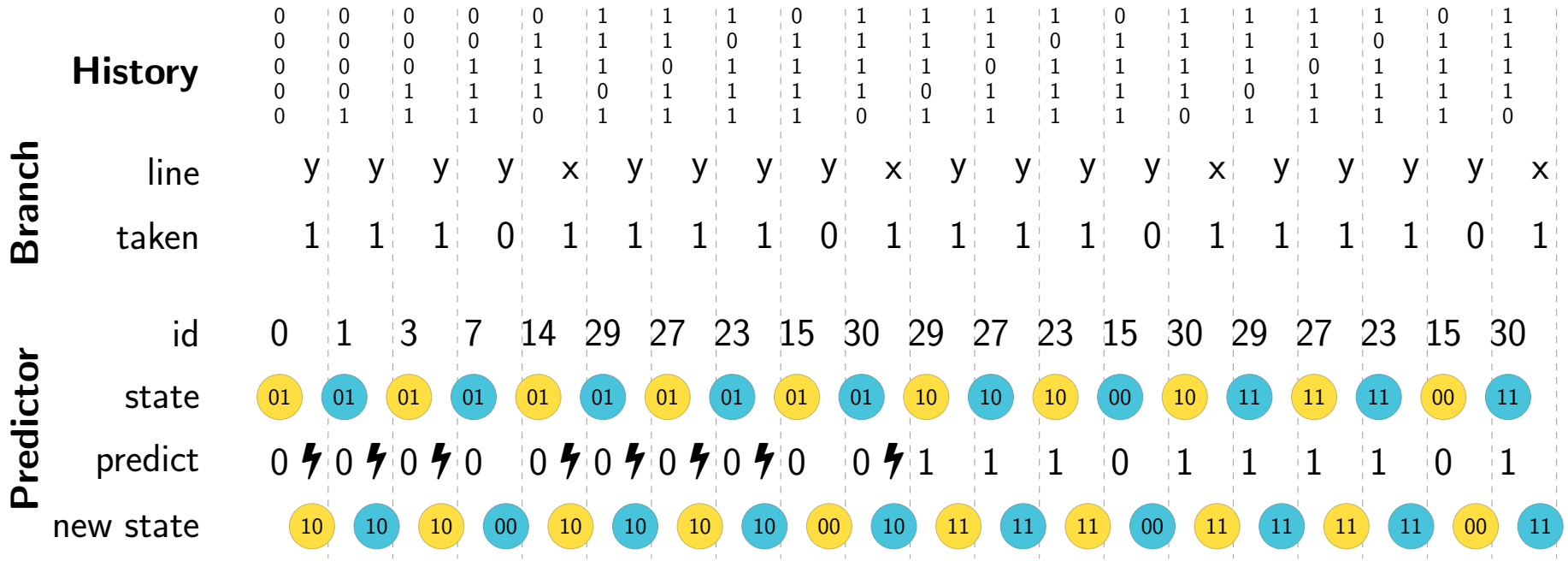

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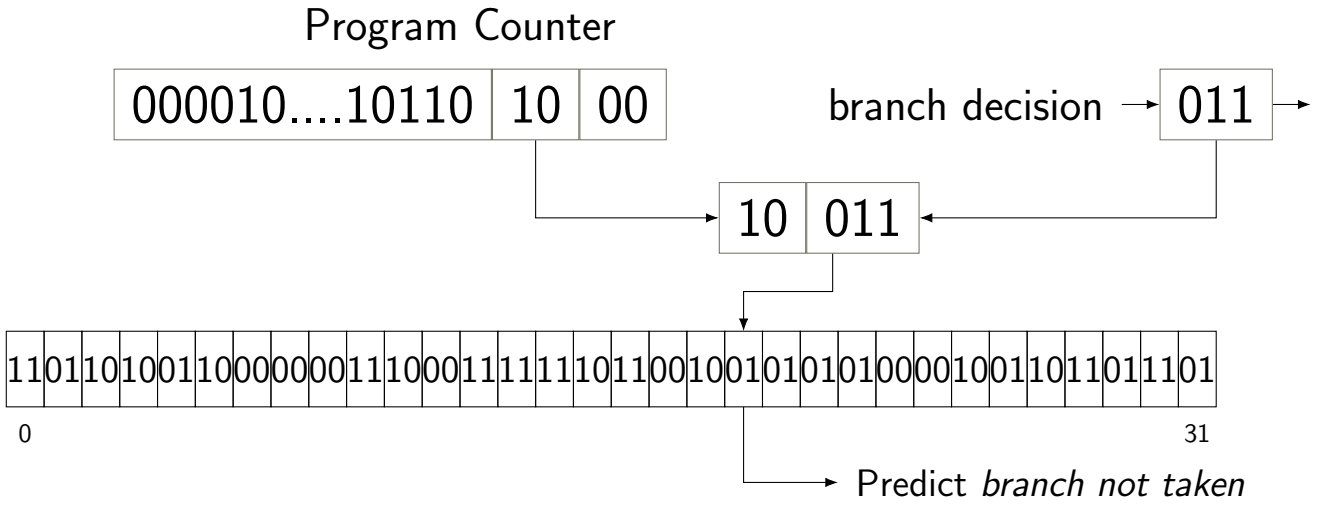

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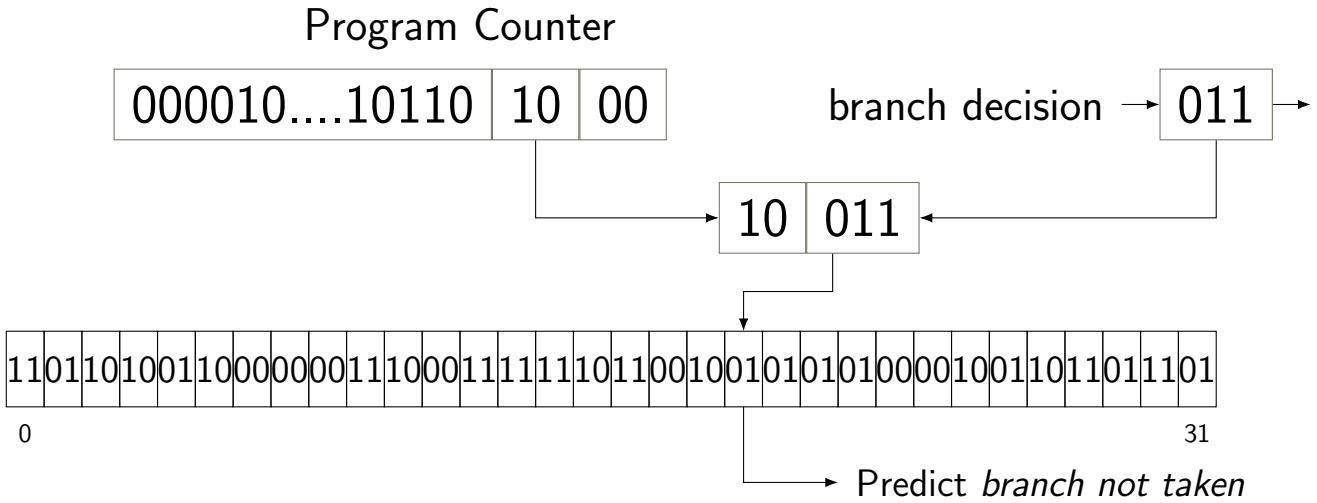

Are we good now?

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0	1	.....	0	.....	0
1	1		1		0
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2-Way Adaptive Local Predictor

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000010....10110	10	00

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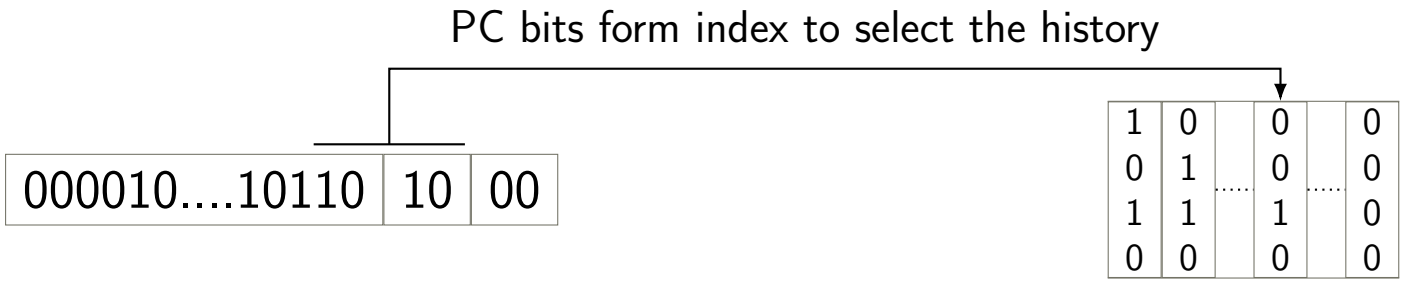

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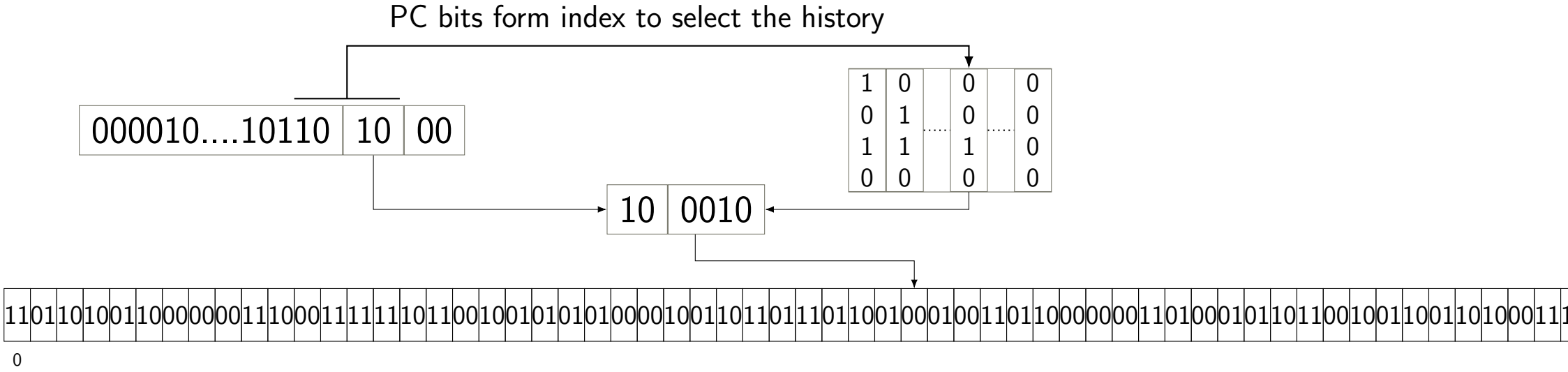

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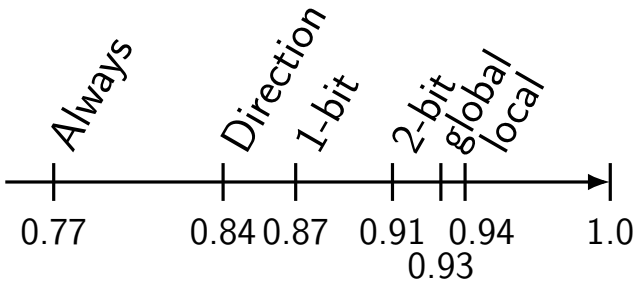

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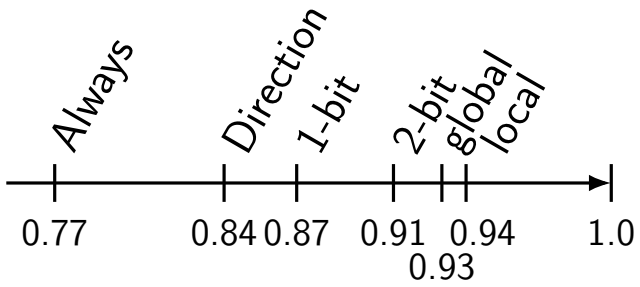

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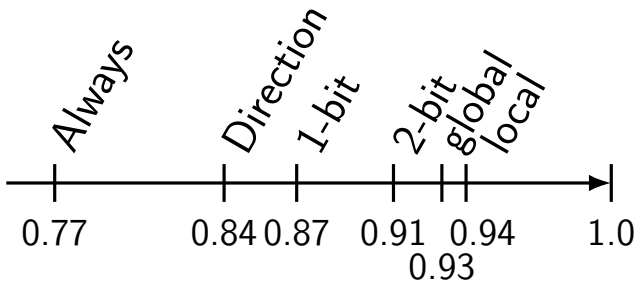

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Modern CPUs incorporate neural network (perceptron-based) branch predictors

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Branch program counter	Last branch target
0x0400ab40	0x0400ab8c
0x04000804	0x0400aaf0
...	...
0x04000800	0x0400440c

Return Address Stack

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0x0400440c

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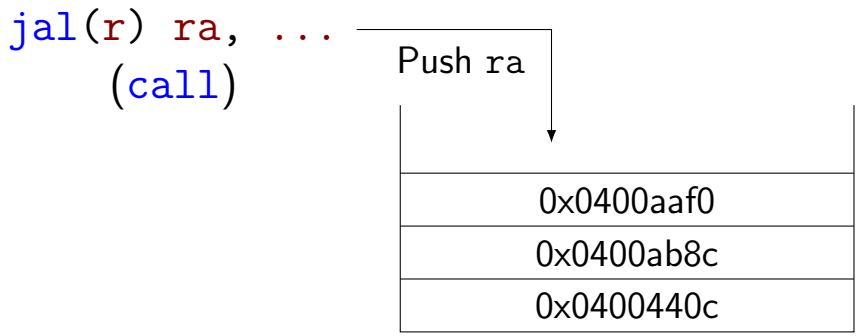
Adding semantics: **Return Address Stack**

- `jalr` as part of function calls (see conventions)
- Idea: Store return address on separate hardware stack



Return Address Stack

Problems with BTB:

- Expensive hardware (content addressable memory), limits entries
- Reduced gain for common function call patterns

Adding semantics: **Return Address Stack**

- `jalr` as part of function calls (see conventions)
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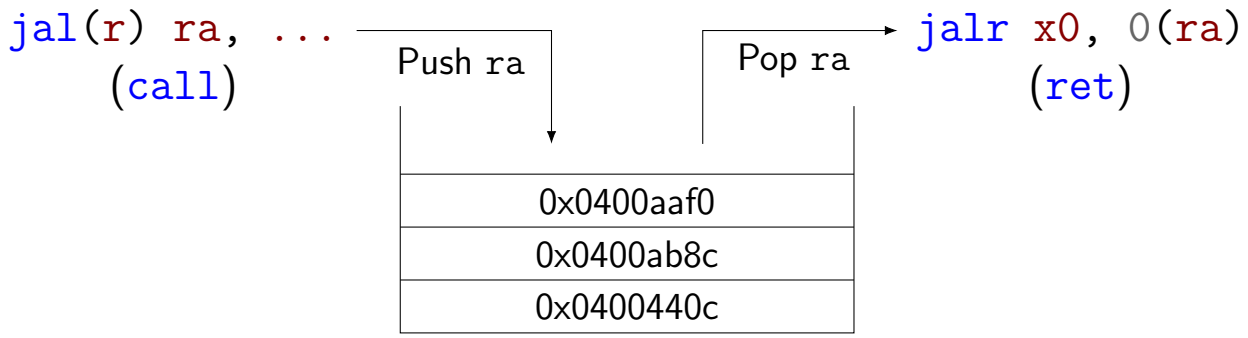

Summary and Learnings

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Difference between predictors and predictor selection