Fakultät für
Informatik und
Mathematik

HOCHSCHULE
FÜR ANGEWANDTE
WISSENSCHAFTEN
MÜNCHEN

COMPUTER ARCHITECTURE

Chapter 4 – Complex Pipelining

Prof. Dr.-Ing. Stefan Wallentowitz

Department 07 – Munich University of Applied Sciences

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Course Organization

GPU

[rwindr, Pixabay]

PCIe

Peripherals

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SATA

[WallpaperSafari, Public Domain]

FSB

[Intel DE, CC BY-SA 2.0]

South Bridge

North Bridge

Central Processing Unit (CPU)

[George Hodan, CC0]

USB

DDR

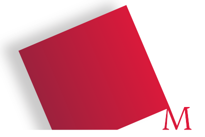
Caches

- Basics
- Pipelining
- Compley Pipelining

[Martyx, CC BY-SA 3.0]

Main Memory

Course Organization



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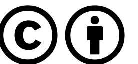
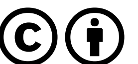


Pipeline Optimizations



Pipeline Optimizations

Goal: Bring IPC up (near to one or even above)

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Speculative Execution

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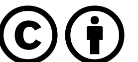

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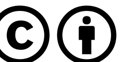

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- Instruction Level Parallelism (ILP)

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  - Execution of multiple different instruction streams

Recap: Pipelining

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Assumption: Each instruction takes one cycle per stage

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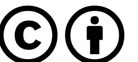
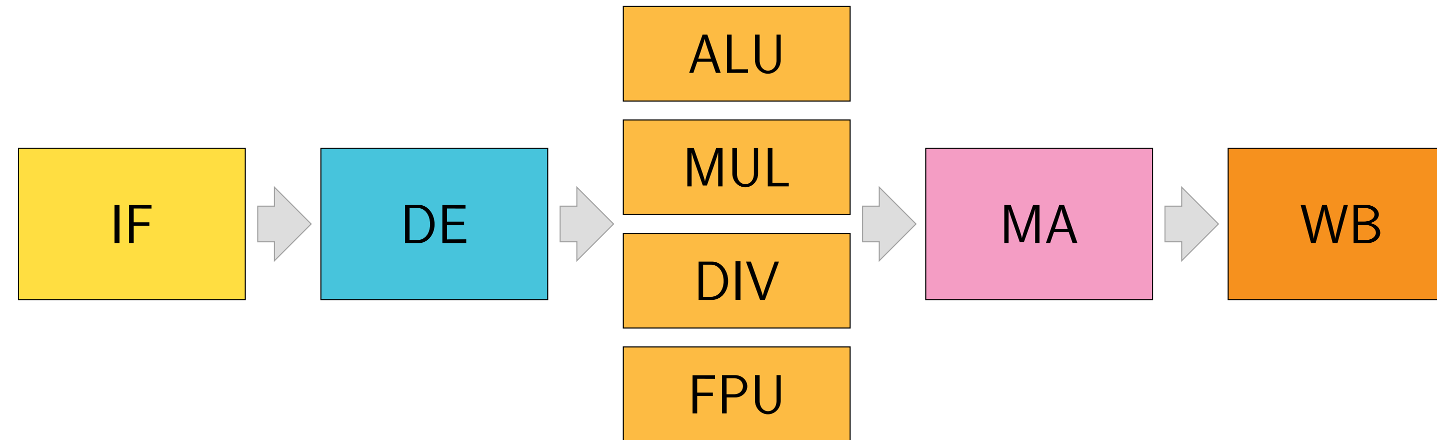
Pipeline: Functional Units

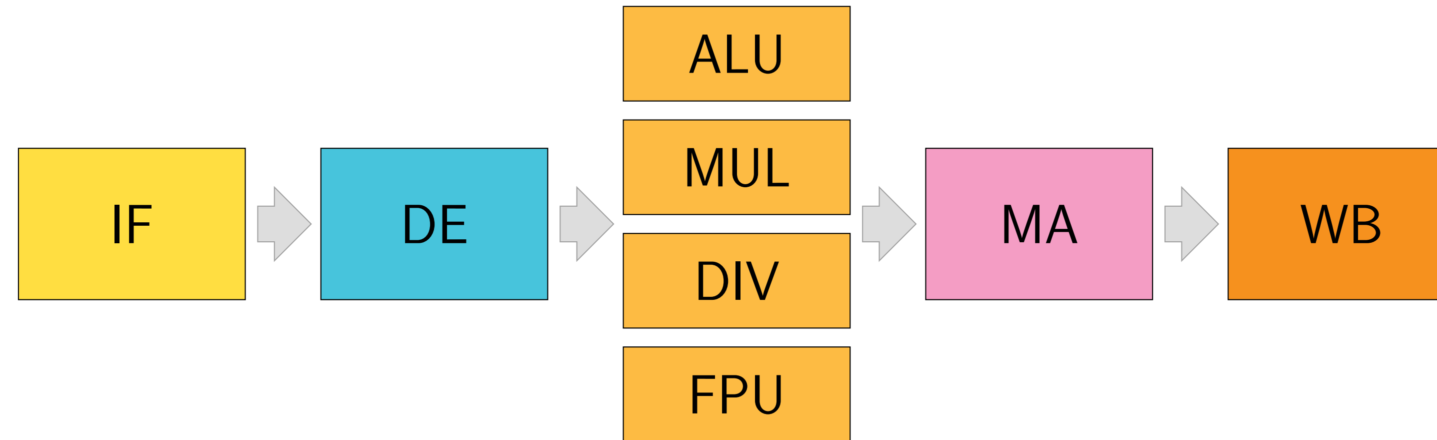


Pipeline: Functional Units



Split EX into functional units (FU): Different hardware building blocks

Pipeline: Functional Units



Split EX into functional units (FU): Different hardware building blocks

Multicycle instructions: Instructions don't complete in one cycle:
Multiplier, Divider, Floating Point Unit (FPU)

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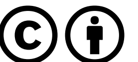
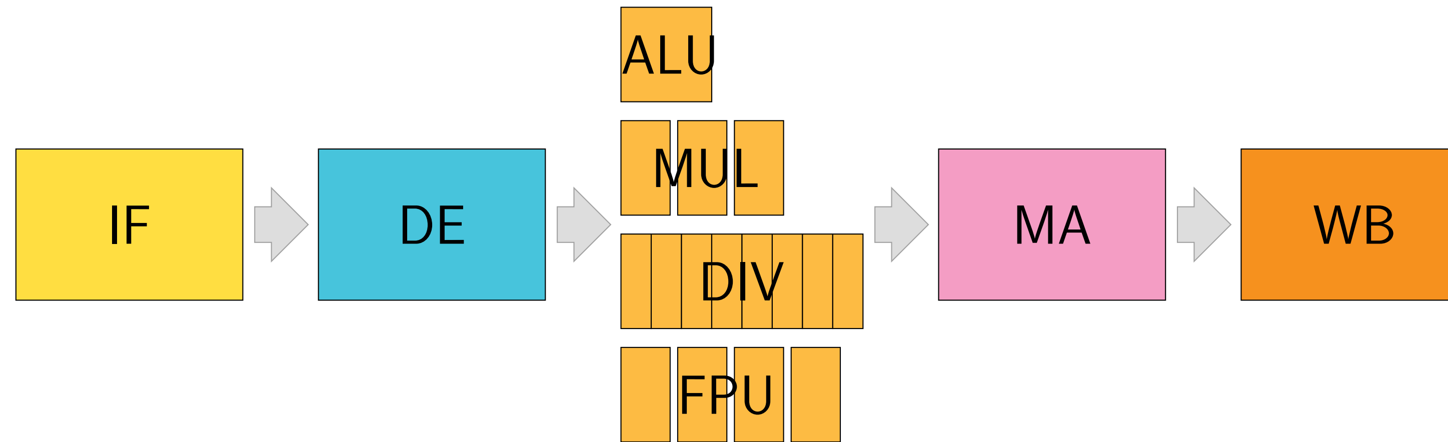
Functional Units: Multicycle Pipelining

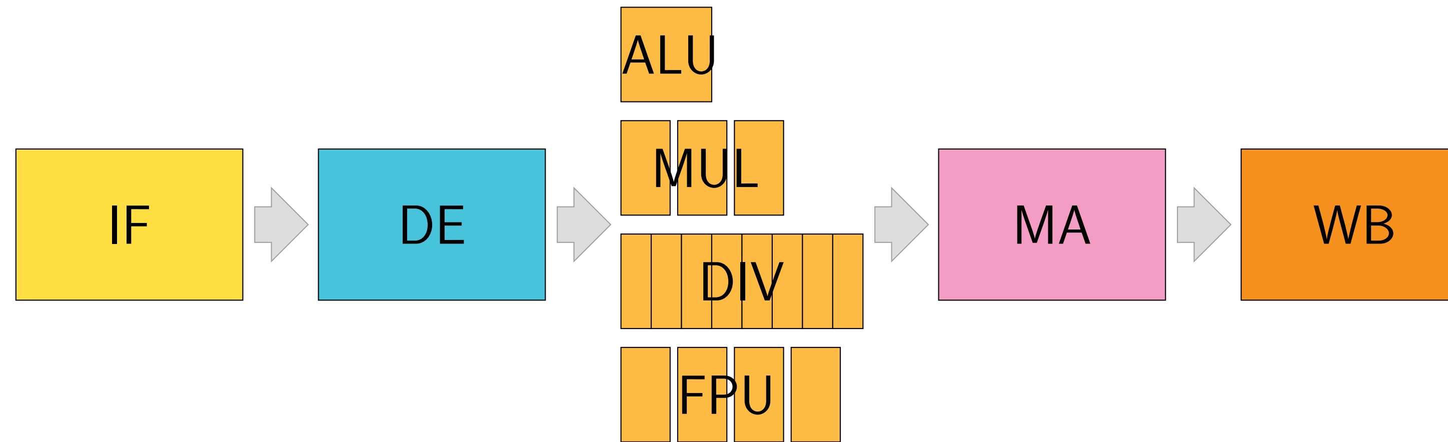


Functional Units: Multicycle Pipelining



Multicycle FUs may be pipelined: Decomposition of operation

Functional Units: Multicycle Pipelining



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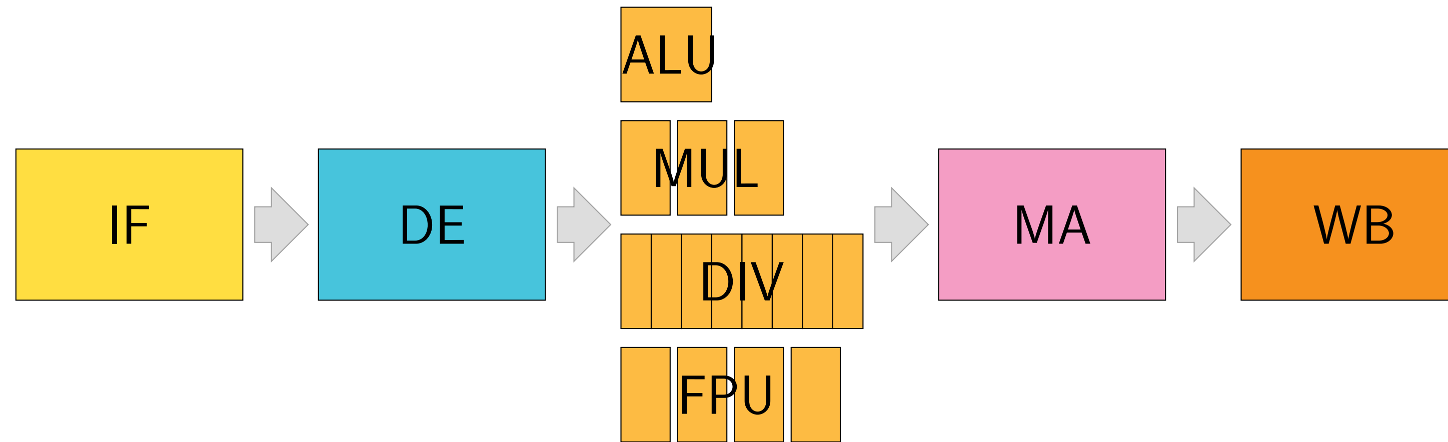

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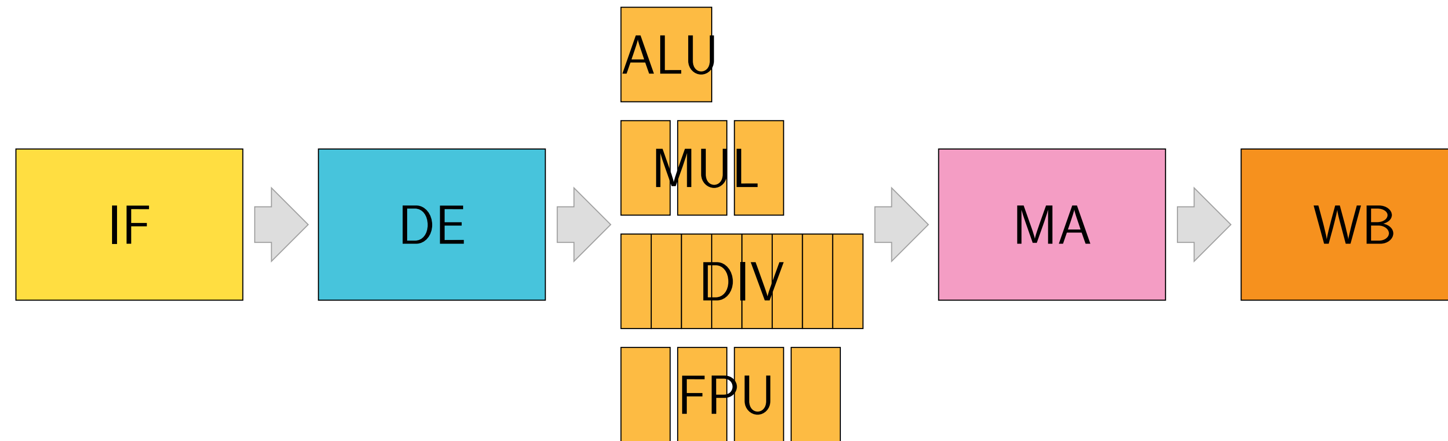


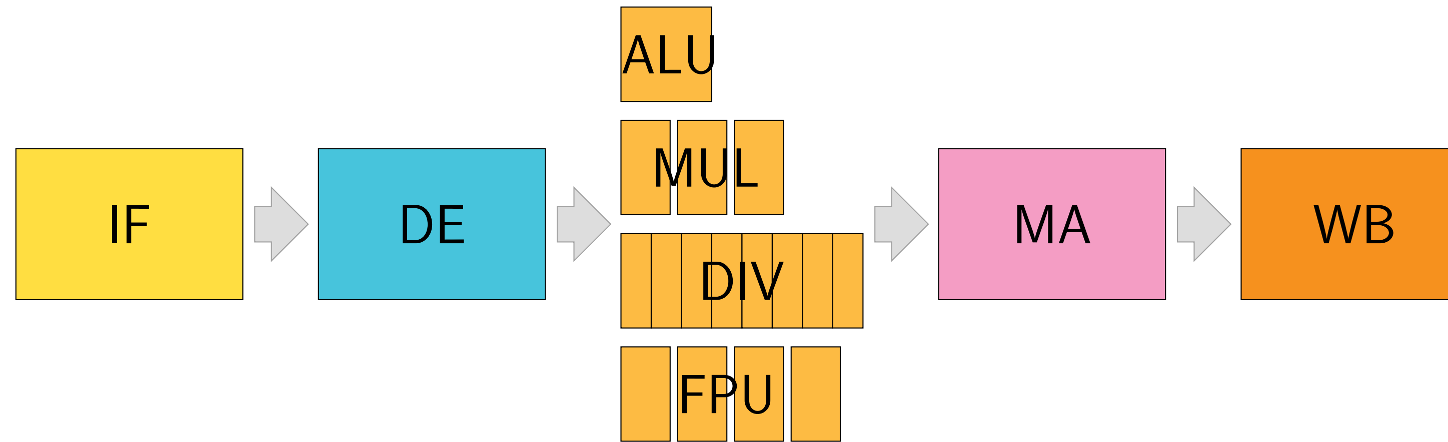
Multicycle FUs may be pipelined: Decomposition of operation

Sometimes not possible: DIV often shares one unit over multiple cycles

Allows for parallel execution of multiple instructions in one FU (not always the case)

(note: In the diagram each block corresponds to one clock cycle, differently scaled)

Multicycle Metrics



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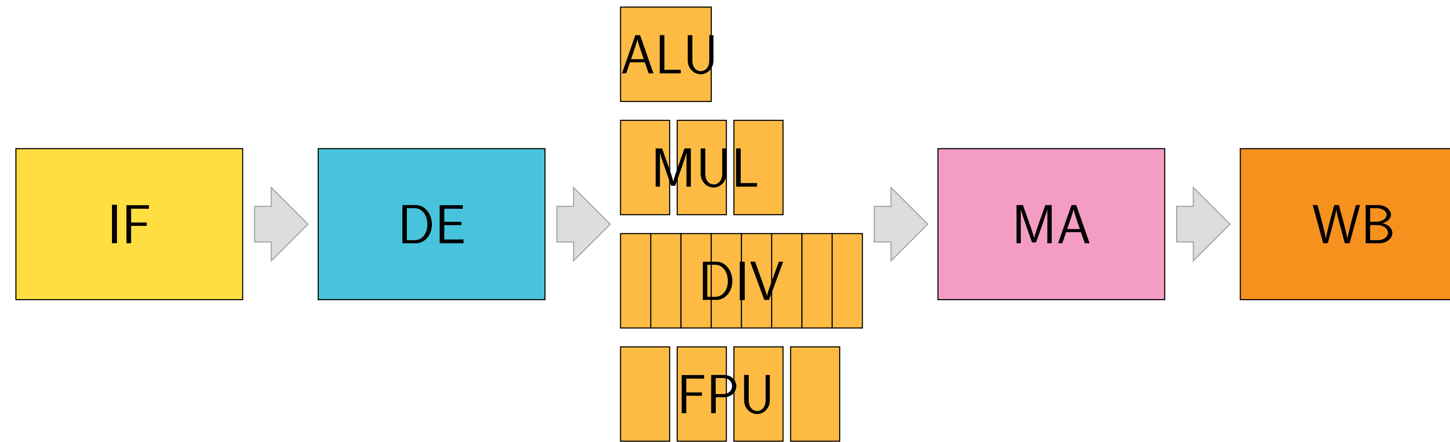
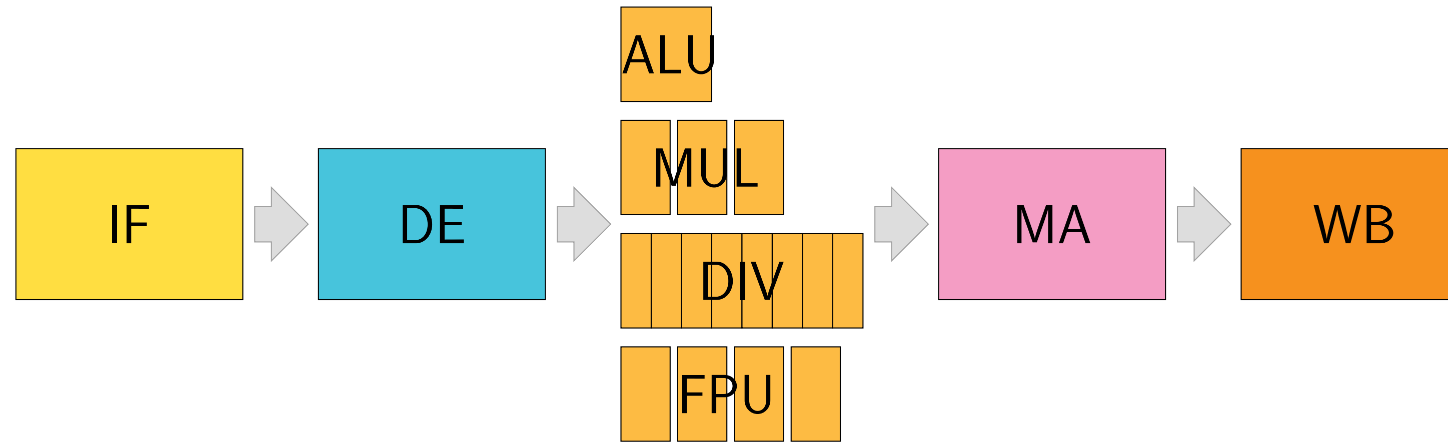


Latency

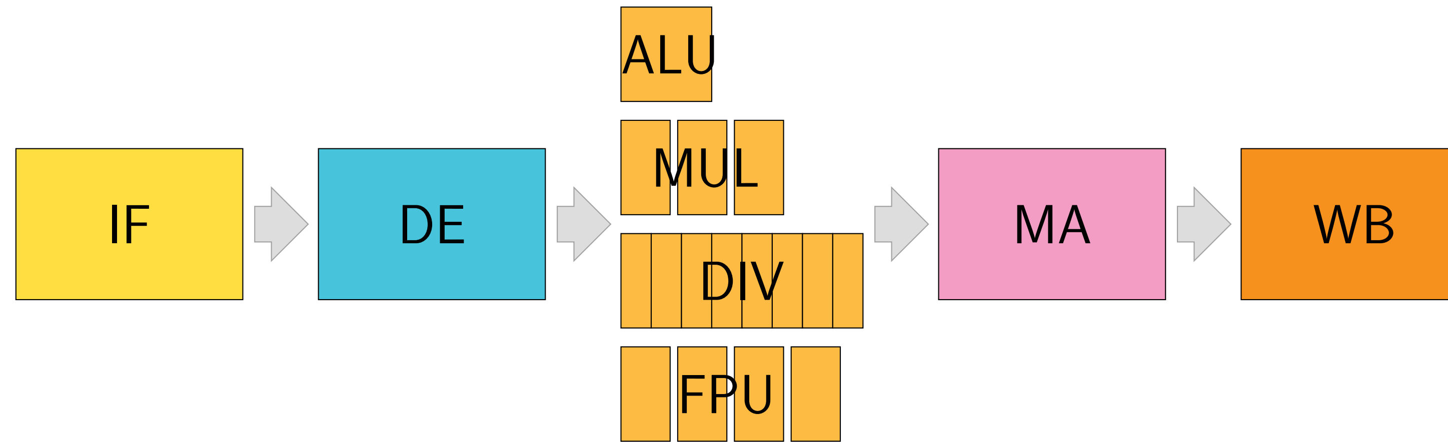
Multicycle Metrics



Latency

- Minimal time for instruction to traverse a functional unit

Multicycle Metrics



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Initiation Interval

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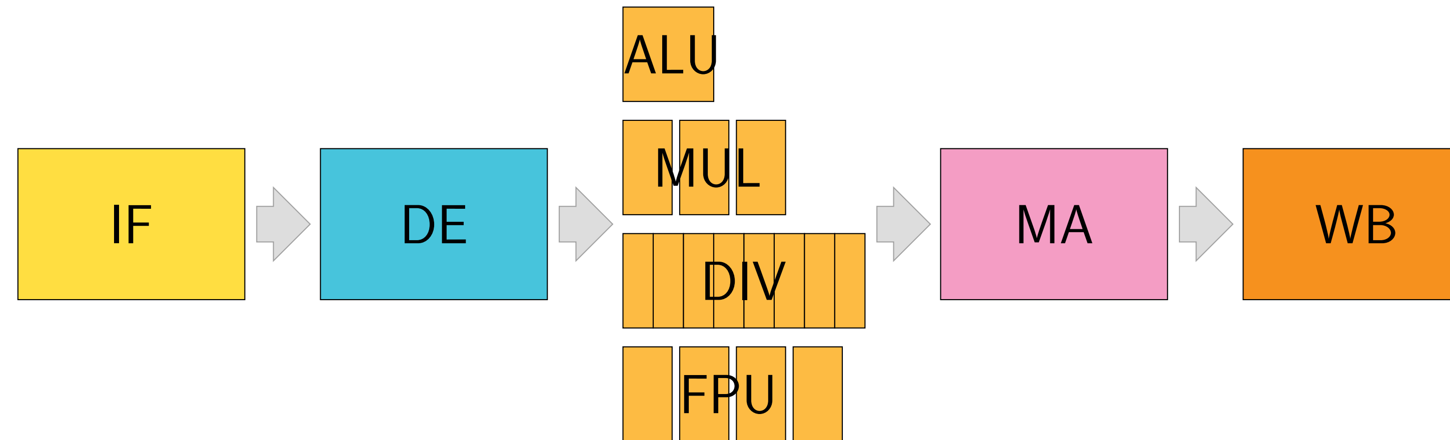
Multicycle Metrics



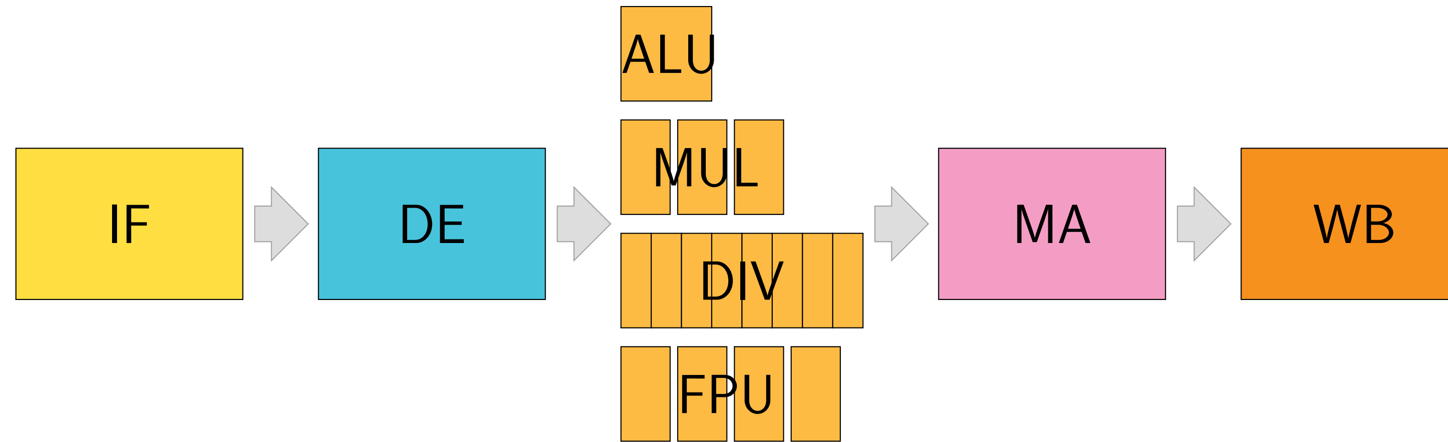
Latency

- Minimal time for instruction to traverse a functional unit

Initiation Interval

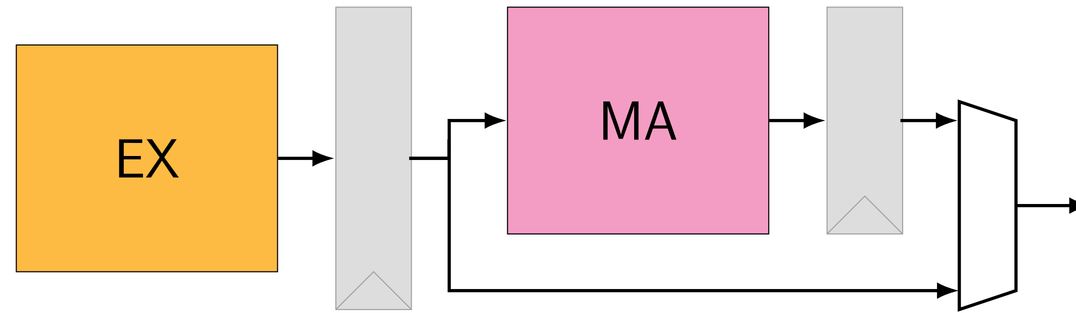
- Minimal duration between two instructions can be started in a functional unit

Multicycle Metrics



	Latency	Initiation Interval
(Integer) ALU		
Multiplier		
Divider		
FPU		

Load-Store Access



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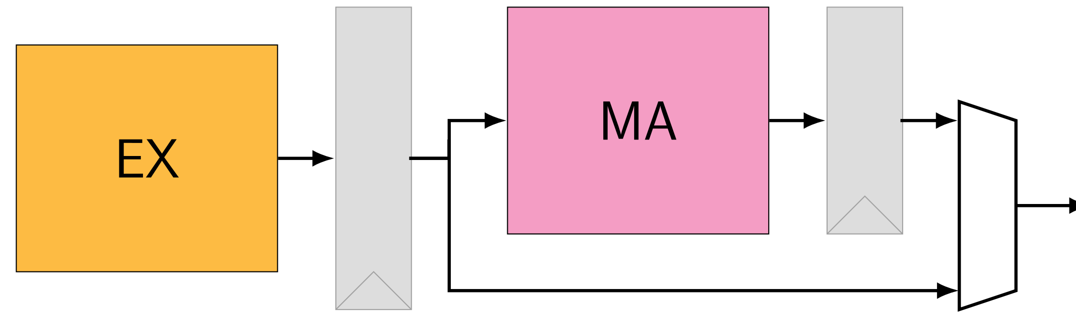
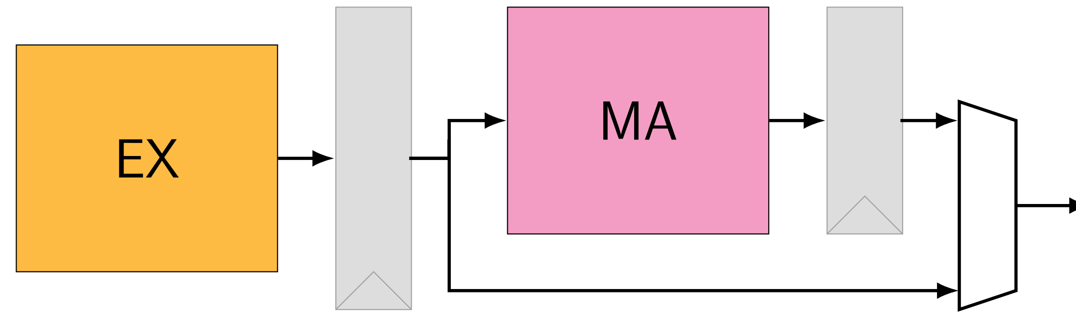
Load-Store Access



Memory access can be optional as most operations don't use it

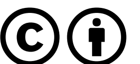
Load-Store Access



Memory access can be optional as most operations don't use it

Specifically after split into functional units

Load-Store Access



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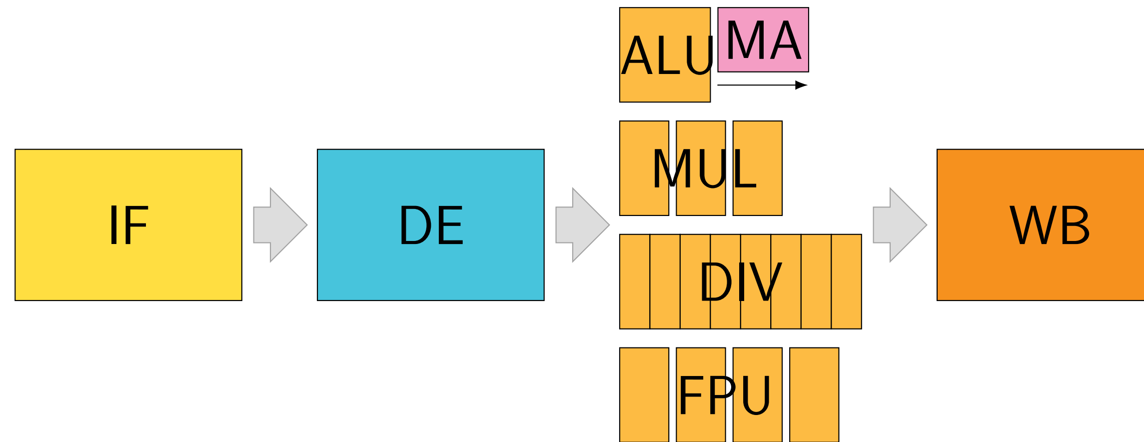
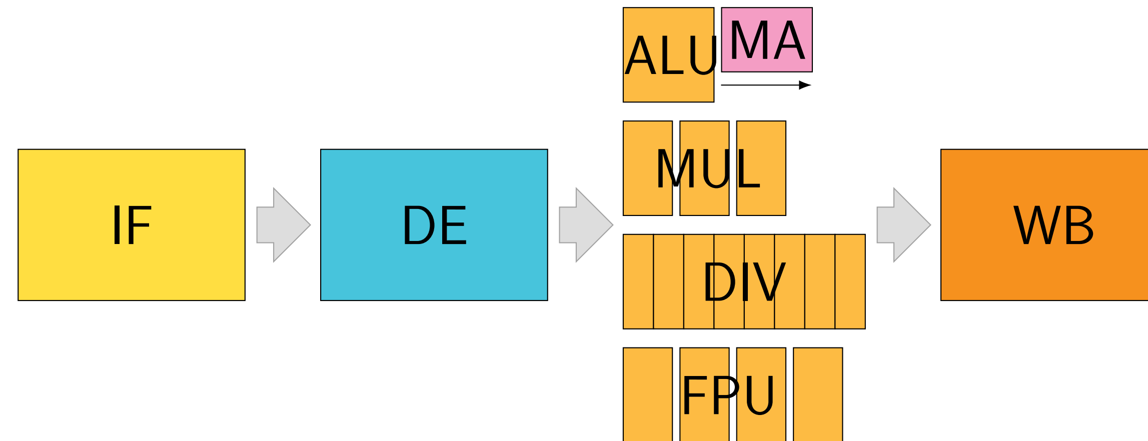


In pipeline with FUs, MA can be an optional extra stage after ALU

Load-Store Access



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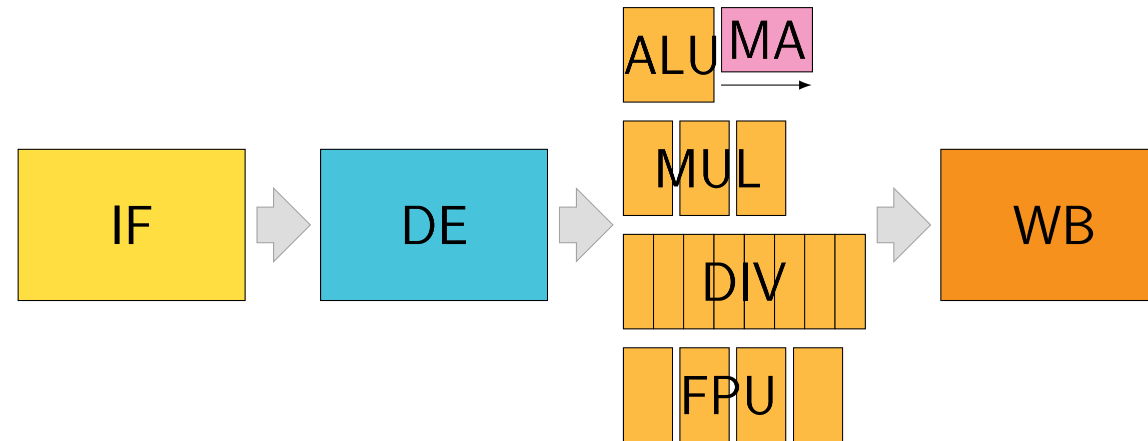

In pipeline with FUs, MA can be an optional extra stage after ALU

- Other paths are not concerned
- For ALU operations its optional to traverse MA

Example: Only one instruction in FUs

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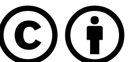
Similar as before: Only one instruction can be in any FU at any time



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Structural hazard for multicycle operations

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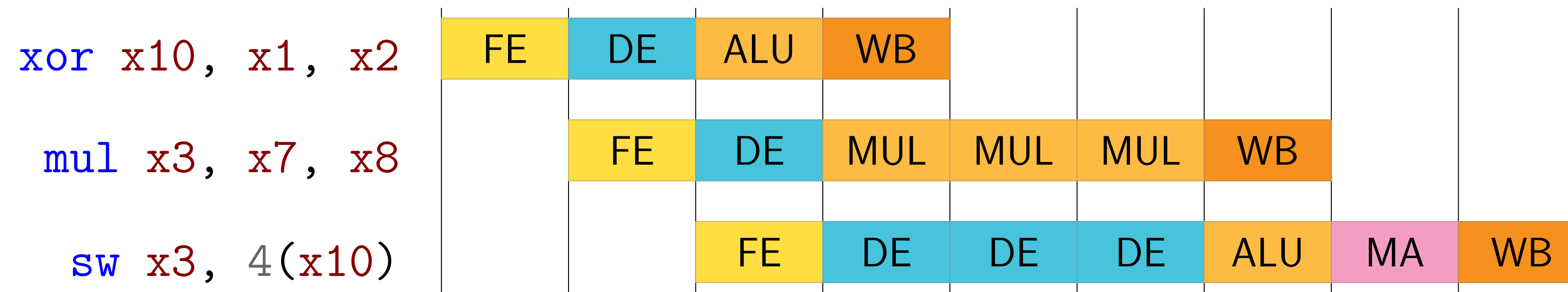
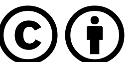
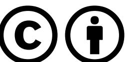


Example: Overlap FU processing



Example: Overlap FU processing

Issue at most one instruction per cycle



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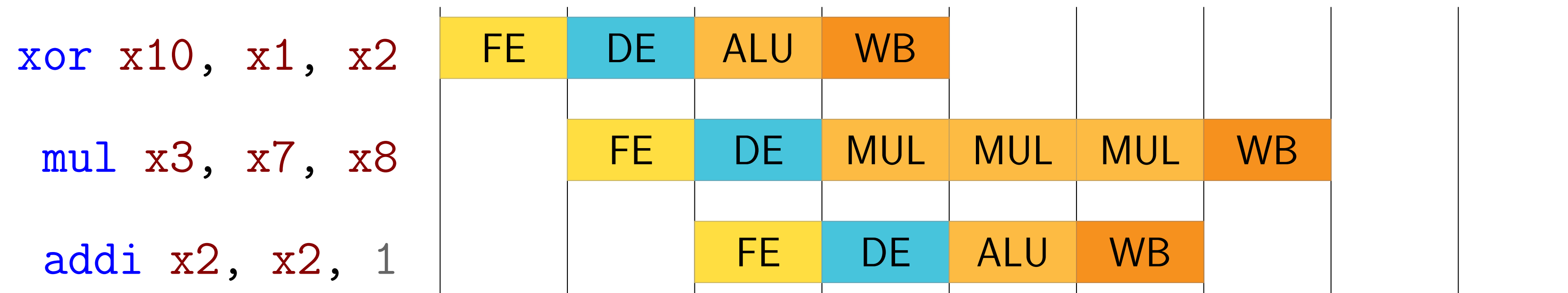
But: multicycle instructions may still be ongoing



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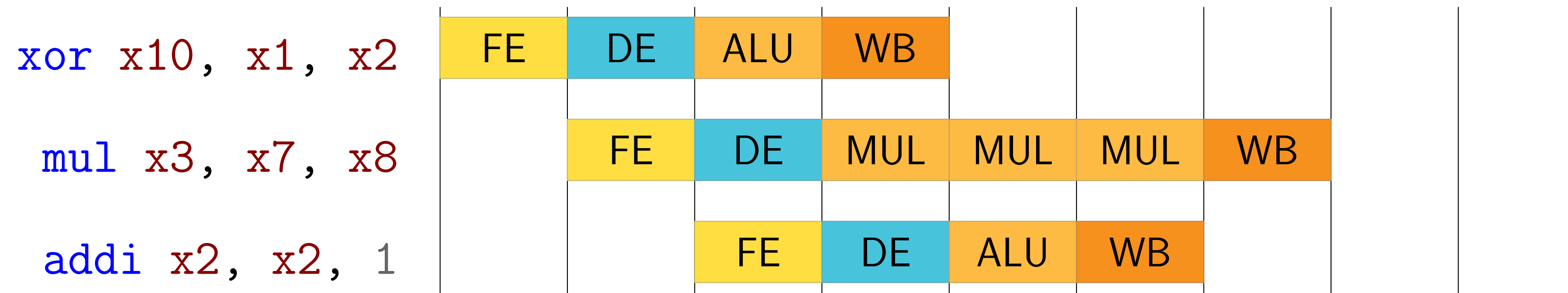
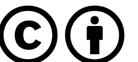


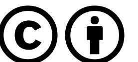
Due to different latency: Instructions can "overtake" others

Out-of-Order Completion



Out-of-Order Completion

Even when started in correct order, instructions can complete *out-of-order*



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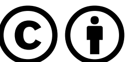
Structural hazard on writeback stage, can be resolved



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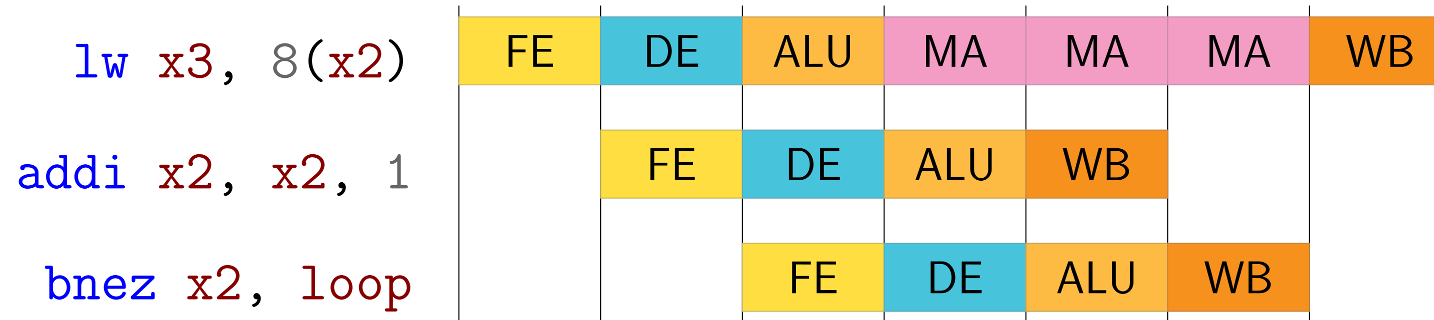

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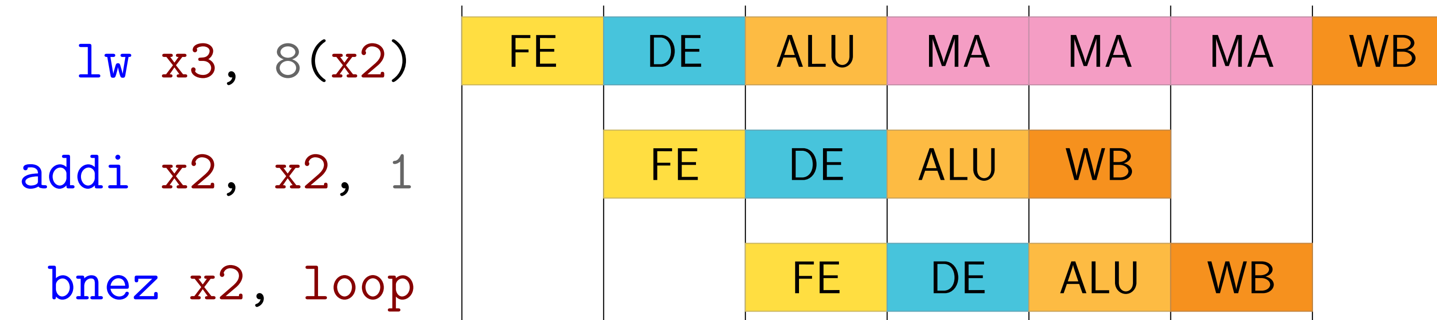

Problems?

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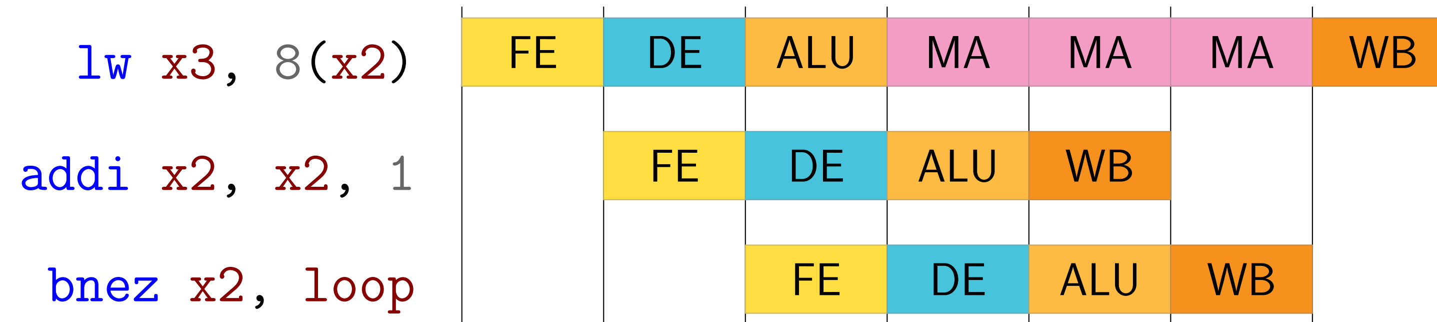
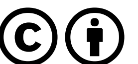


Problems?

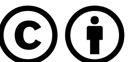
- What when there is an exception with the load?
- Example: Access fault, handled by OS, then continue

Out-of-Order Completion: Exception



Out-of-Order Completion: Exception

Problem:



Out-of-Order Completion: Exception

Problem:

- Following instructions completed when load exception occurs

Out-of-Order Completion: Exception

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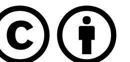
- `addi` and `bnez` will be executed again, functional error



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- Imprecise exceptions: The exception handler needs to clean up

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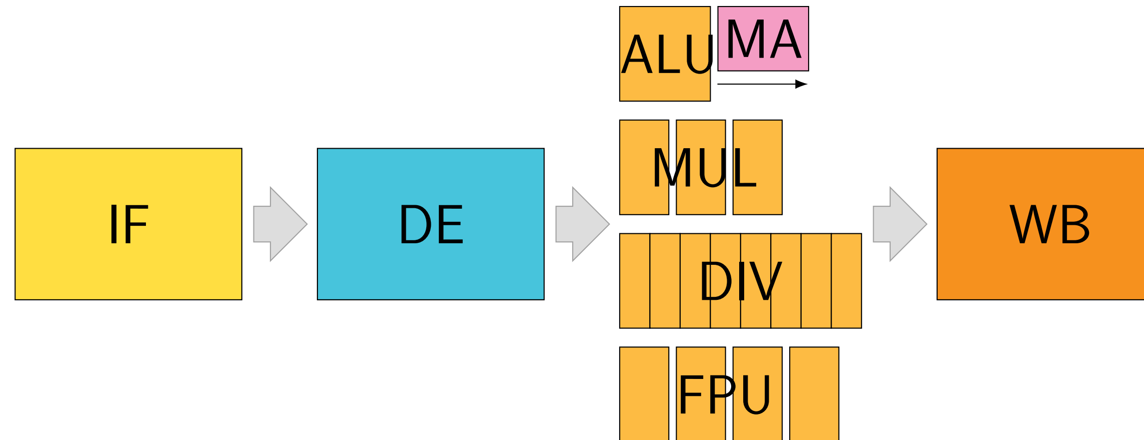
Potential solutions

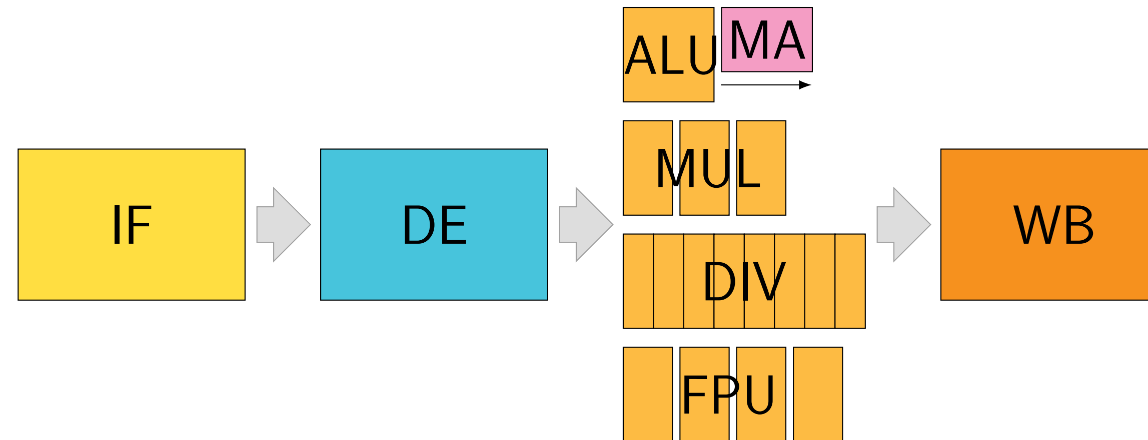
- Imprecise exceptions: The exception handler needs to clean up
- Start instruction processing only after sure no exception can occur
- Buffer results and commit in correct order (forwarding needs to look there too!)

Re-Order Buffer



Re-Order Buffer

Split between instruction *retire* and architectural *commit*



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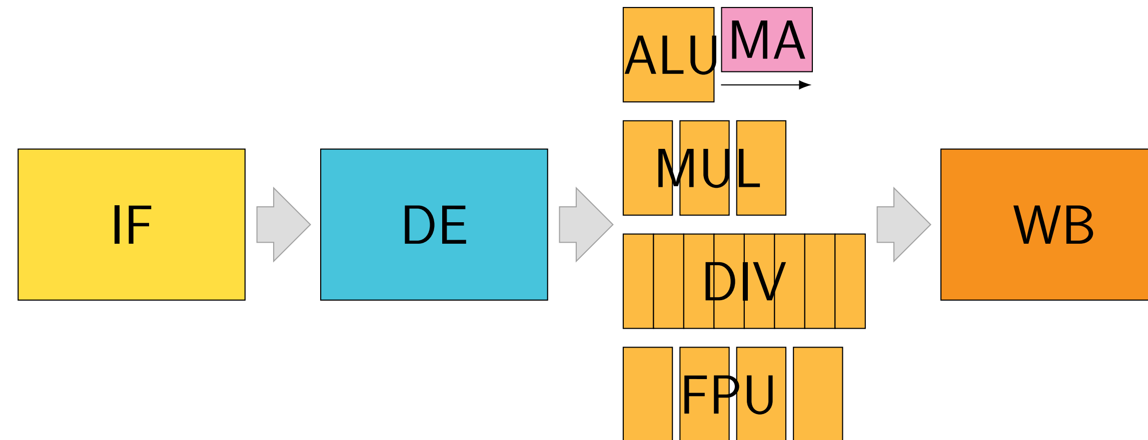
Re-order buffer (ROB) buffers results after out-of-order retire, commits in-order



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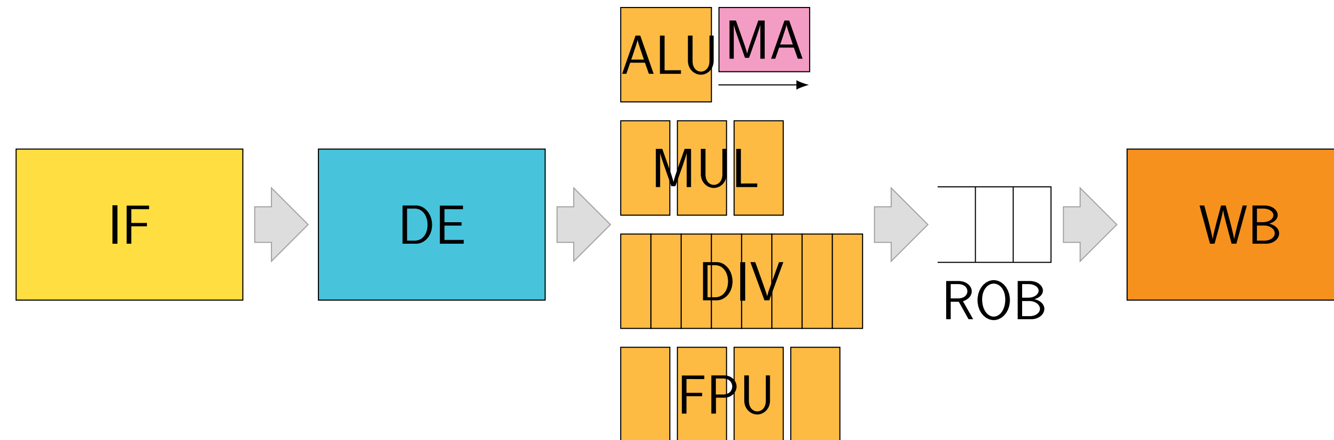
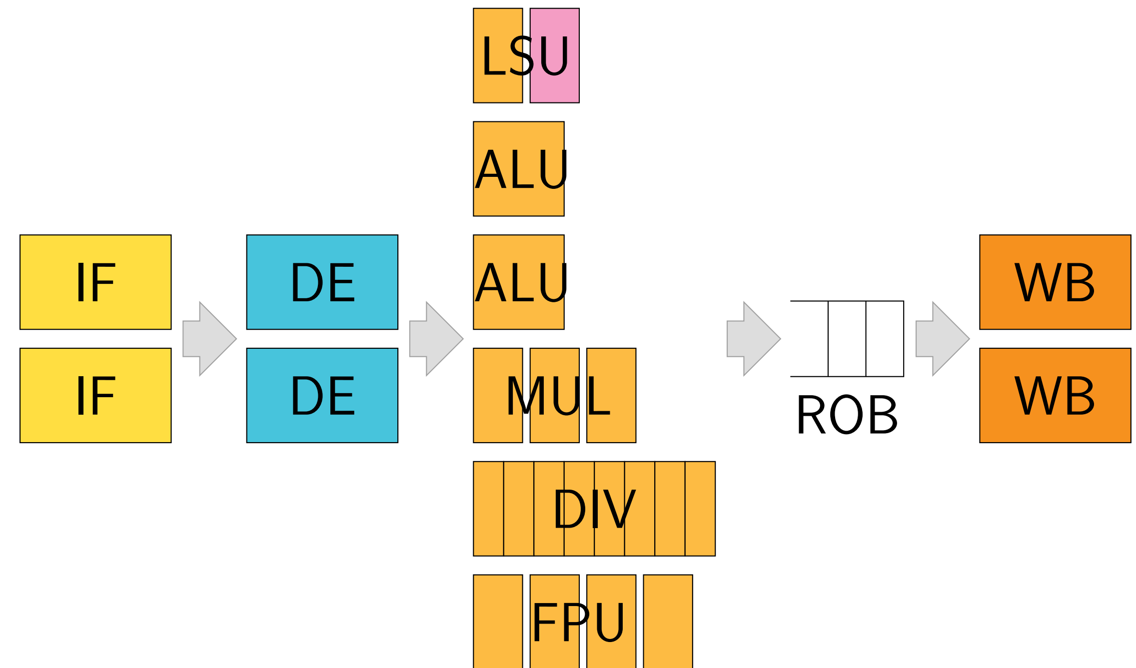
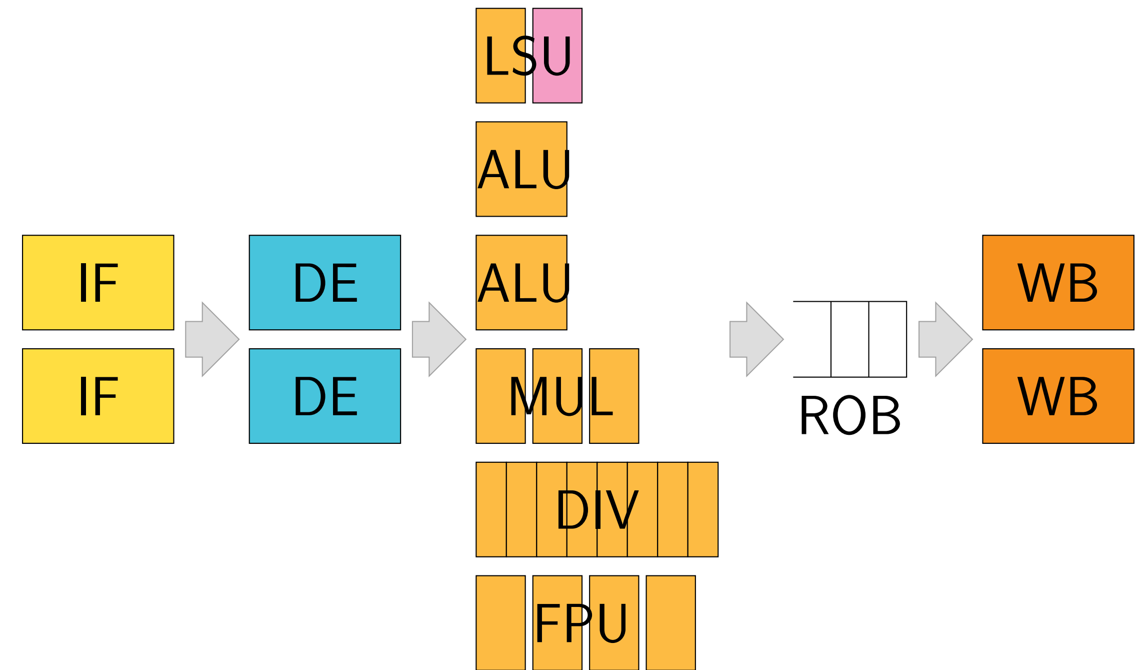


Superscalarity



Superscalarity

Execute multiple instructions in parallel



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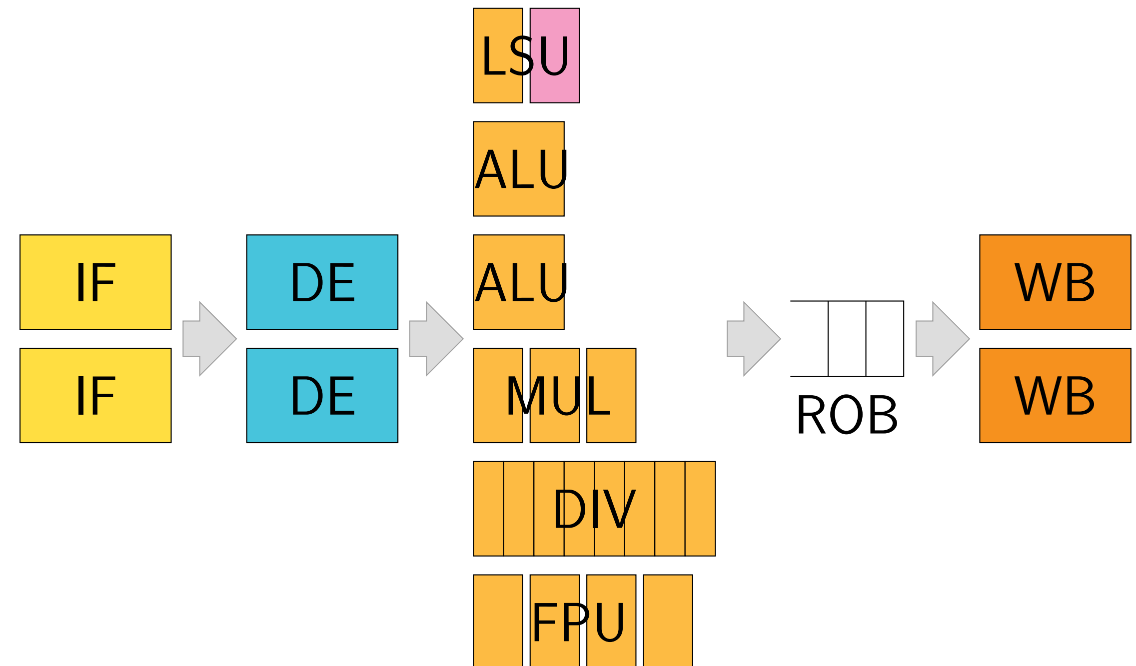
Execute multiple instructions in parallel

Usually: replicate FUs



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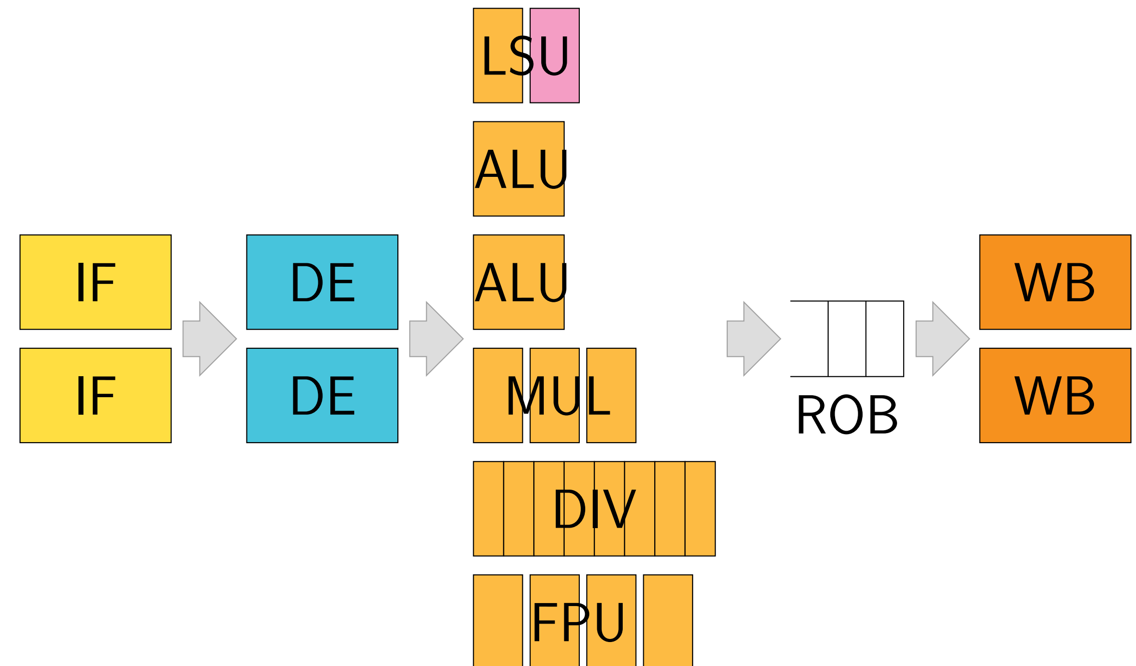

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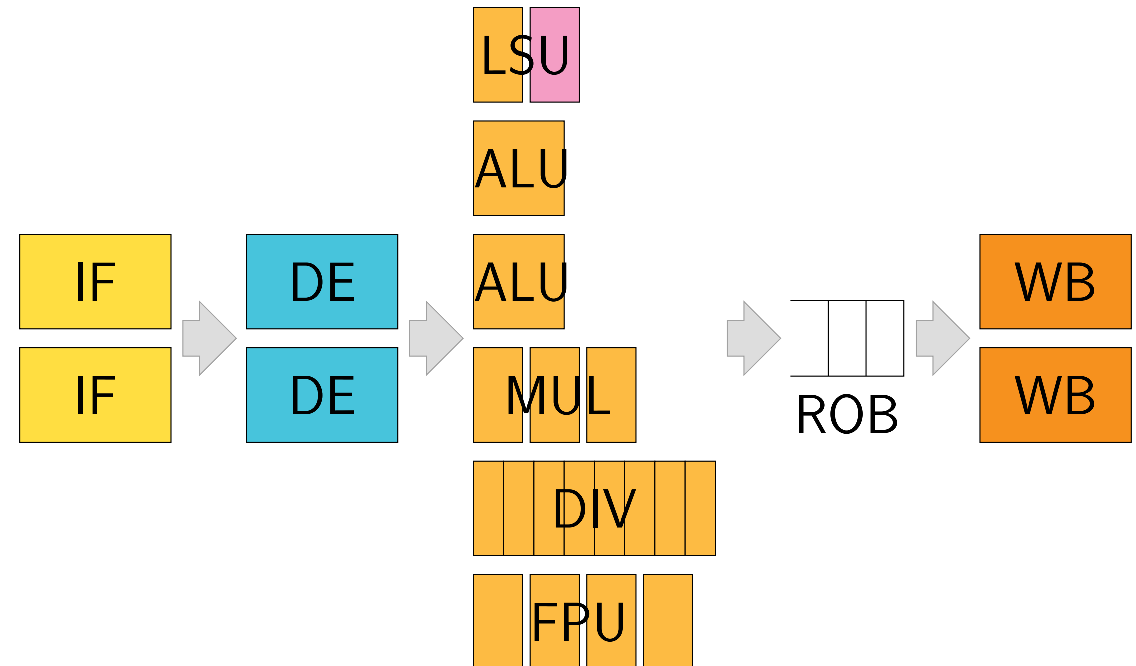

Superscalarity

Execute multiple instructions in parallel

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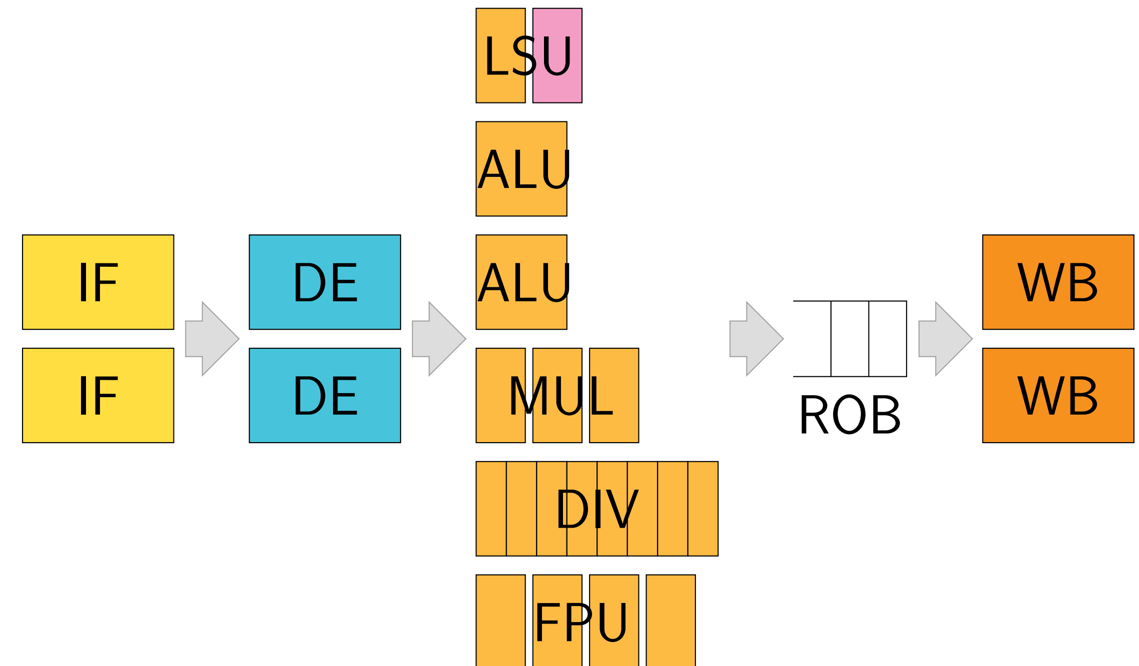
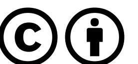
- LSU as separate FU

Increases theoretical IPC by number of parallel instructions (**issue width**, here: 2)



Superscalarity: Example



Superscalarity: Example

Exploit instruction level parallelism

Instruction	1	2	3	4	5	6	7	8	9
`xor x10, x1, x2`	FE	DE	ALU	ROB	WB				
`addi x13, x13, 1`	FE	DE	ALU	ROB	WB				
`mul x3, x7, x8`		FE	DE	MUL	MUL	MUL	ROB	WB	
`addi x2, x2, 1`		FE	DE	ALU	ROB	ROB	ROB	WB	

Superscalarity: Example

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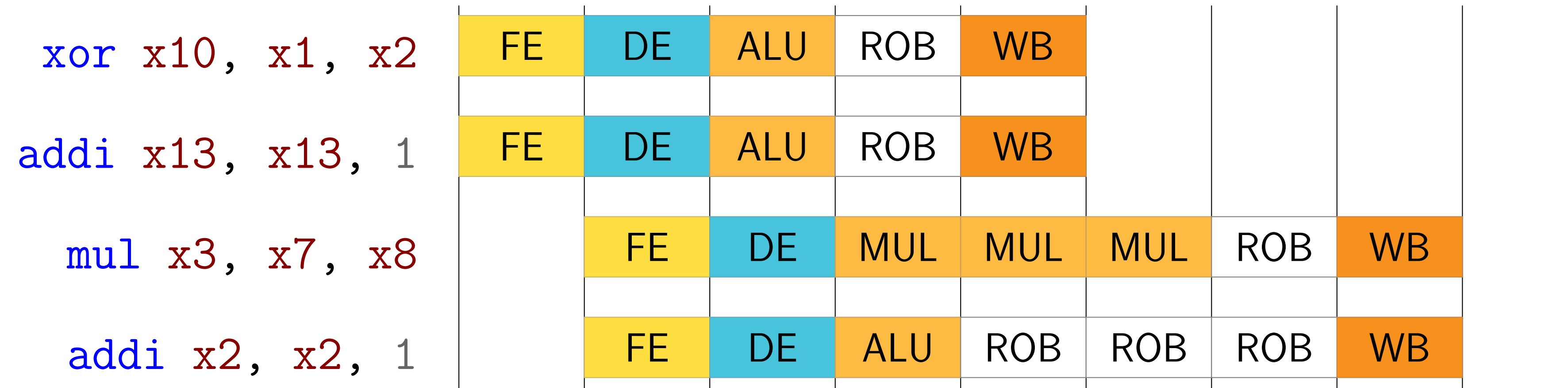

Need issue width at each part of the pipeline, otherwise limits speedup

Superscalarity: Example

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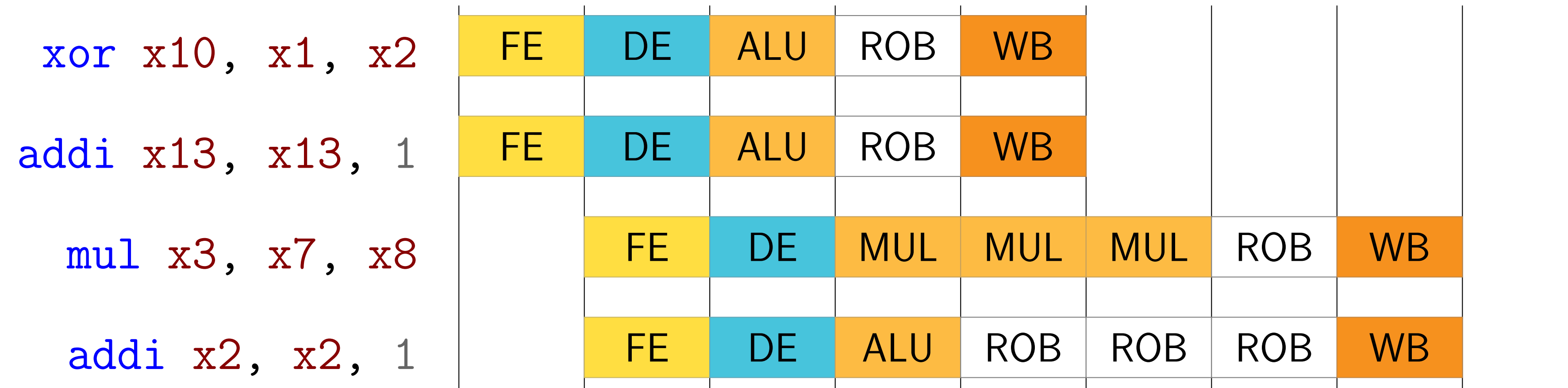
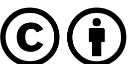
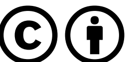


Need issue width at each part of the pipeline, otherwise limits speedup

Instruction stream split obvious here, but how do we schedule instructions in general?

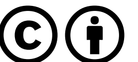


Instruction Scheduling



Instruction Scheduling

Scheduling: Select instructions to be started in EX stage



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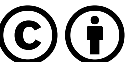

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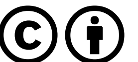
- Need to obey data dependencies



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- Execution of instructions pre-determined

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©ⓘ

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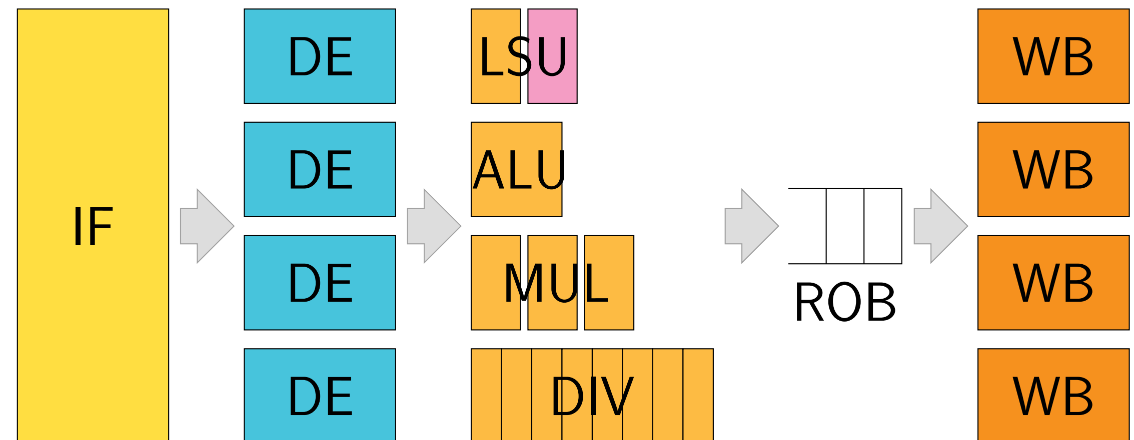
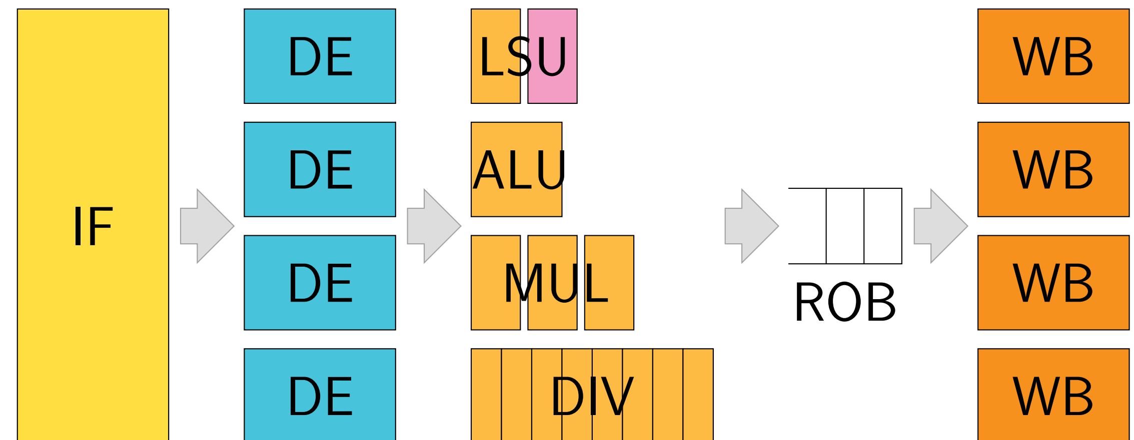
Scheduling and Superscalarity are independent concepts

Static Scheduling: VLIW



Static Scheduling: VLIW

Very Long Instruction Word (VLIW)



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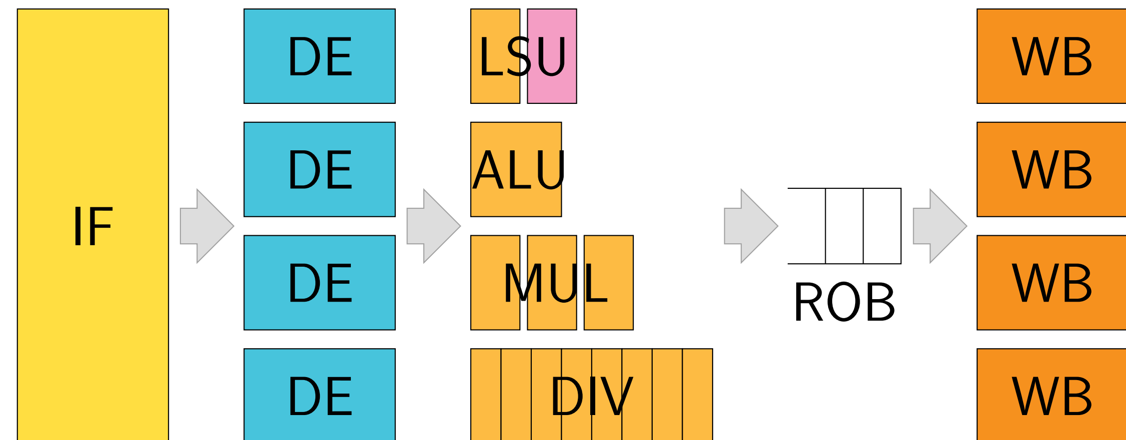
Combine multiple instructions in slots of a long "packet"



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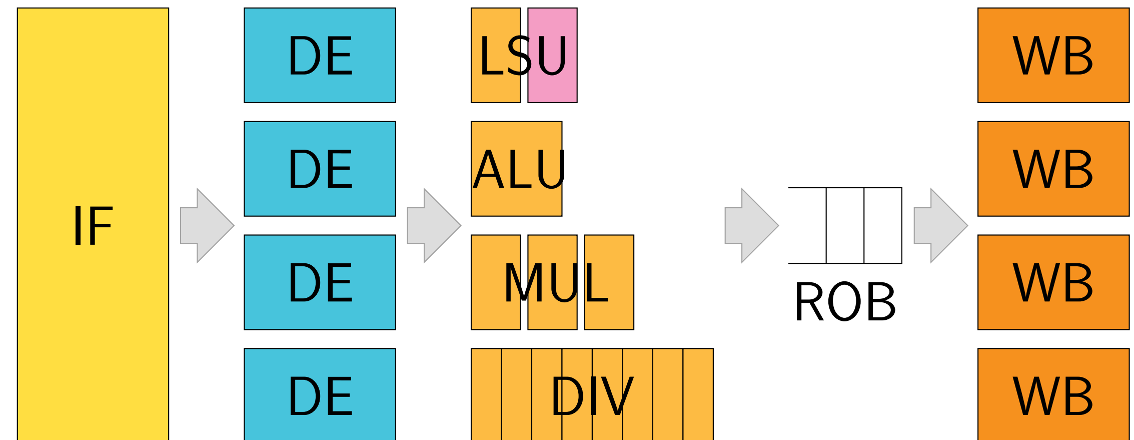

Static Scheduling: VLIW

Very Long Instruction Word (VLIW)

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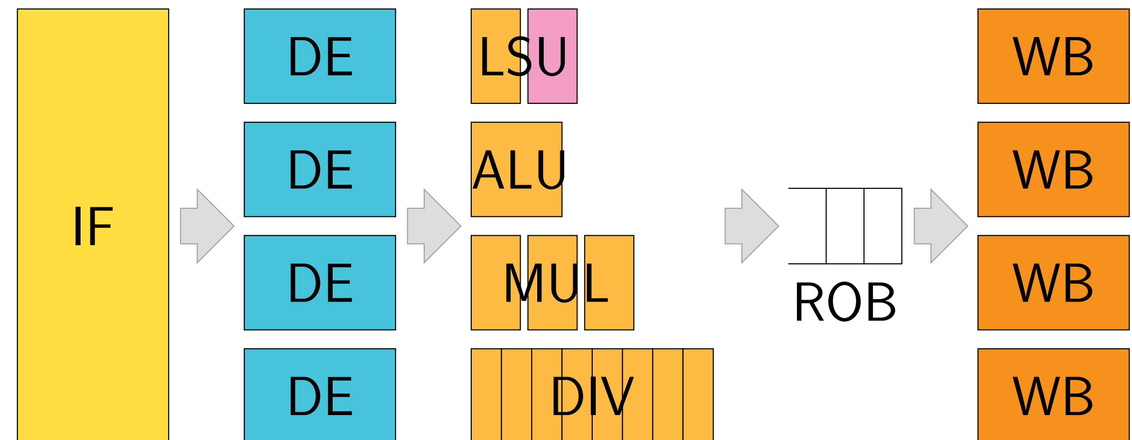
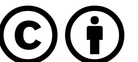
Start complete packet once all instructions in it can be started

Not much hardware overhead, but compilers are hard, challenge: use slots

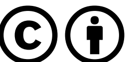


Dynamic Instruction Scheduling



Dynamic Instruction Scheduling

Approach: Start instructions as soon as possible



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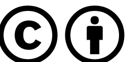
- Once structural hazards are solved: functional unit is free



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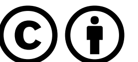
Keep next instruction(s) in buffer

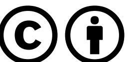
- Instructions are still issued in order (FIFO instruction buffer)
- Where to put it? (IF-DE or DE-EX)

Split the Decode Phase



Split the Decode Phase

Issue



Split the Decode Phase

Issue

- Decode instruction

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- Decode instruction
- Check for structural hazards (can also be instruction buffer full)

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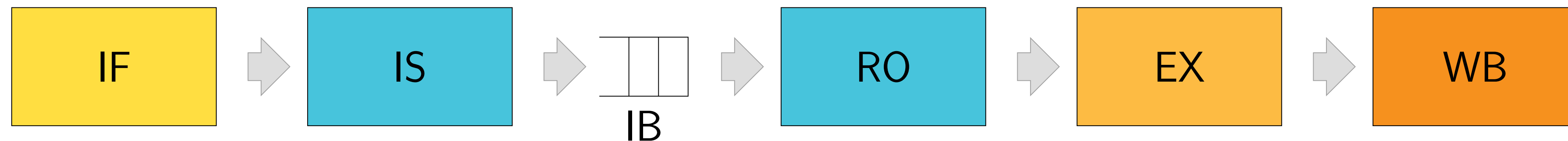
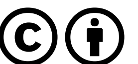
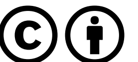


Scoreboard



Scoreboard

Scoreboard: Data structure to track execution



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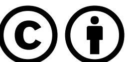
Scoreboard: Data structure to track execution

Keeps all active instructions (in FUs)



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Check current instruction for conflict

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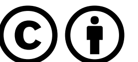
Check current instruction for conflict

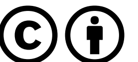
Instruction	FU	rd	rs1	rs2

Scoreboard



Scoreboard

Check scoreboard for every instruction



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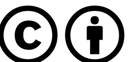
Check scoreboard for every instruction

- Structural hazard: Check if FU can start instruction



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- Start instruction from instruction buffer once no hazards are left, add to SB

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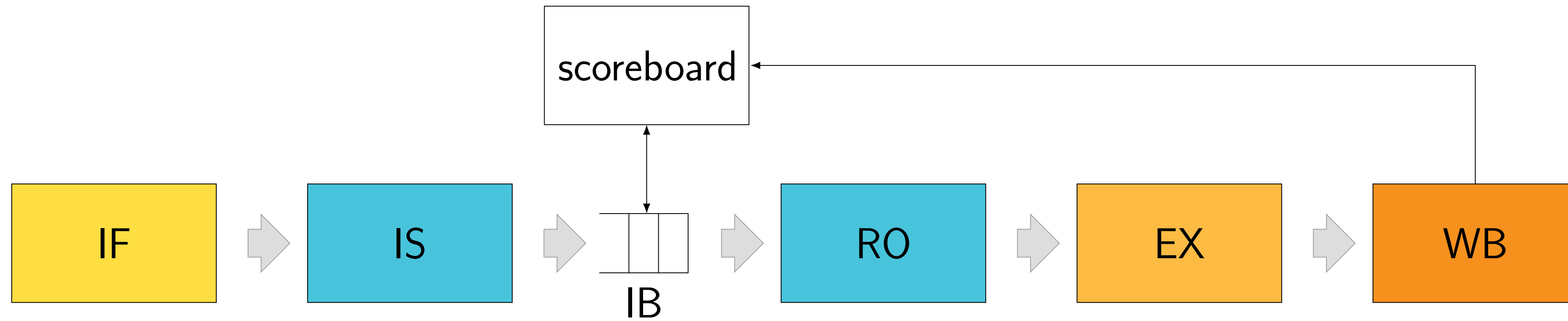
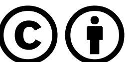
Lifecycle of entries

- Start instruction from instruction buffer once no hazards are left, add to SB
- Remove from SB once result was written

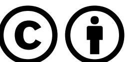
(C) (i)

Scoreboard: Integration



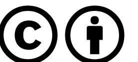


In-Order Scoreboard Scheduling



In-Order Scoreboard Scheduling

Use scoreboard for in-order dynamic scheduling



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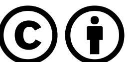
Typical: No bypassing (complexity of many functional units)



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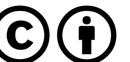

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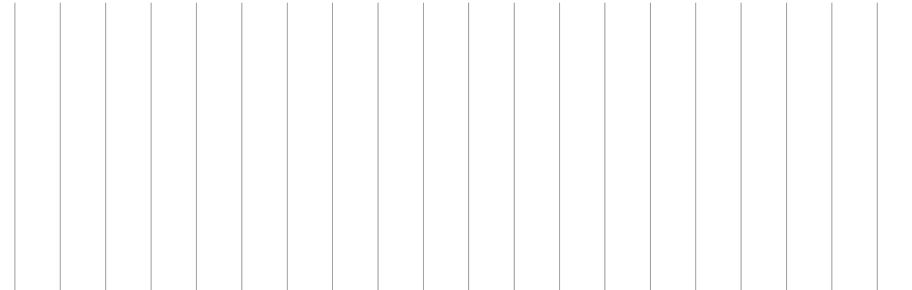
Can we have WAR and WAW for the next instruction?

- **No WAR** as we are in order
- **WAW** can occur, hence need to track destination registers
- We only need to know the pending writes (destination registers)

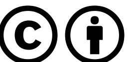
Scoreboard: Example

```
ld x12, 8(x9)
ld x13, 0(x7)
mul x17, x13, x12
subi x18, x12, 2
mul x13, x12, x18
add x10, x17, x13
```

Execution Diagram



Instruction	FU	rd



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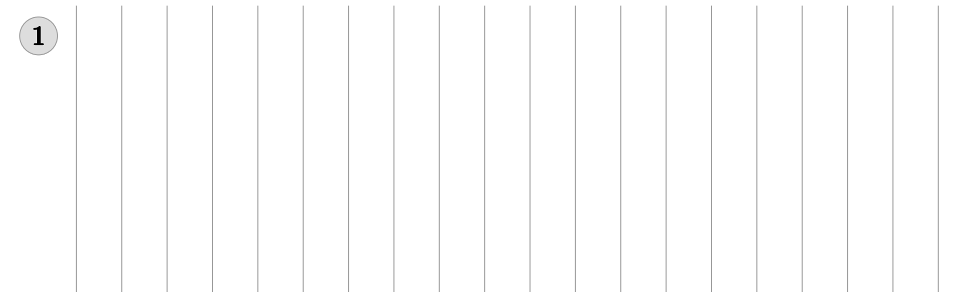
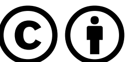


0: #1 can be started



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1 ld x12, 8(x9)
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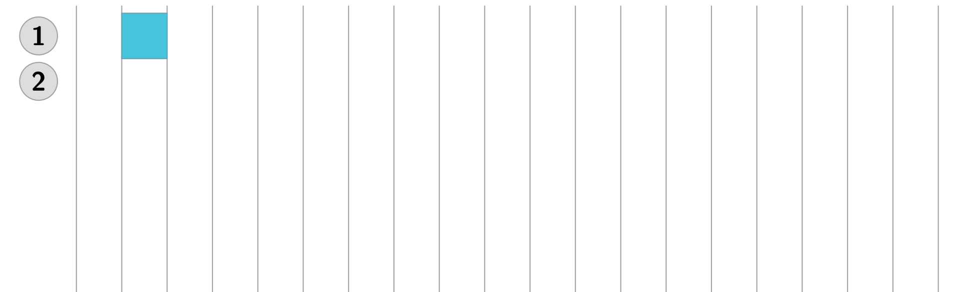
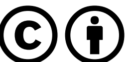


0: #1 can be started
1: #2 can be started, #1 reads operands

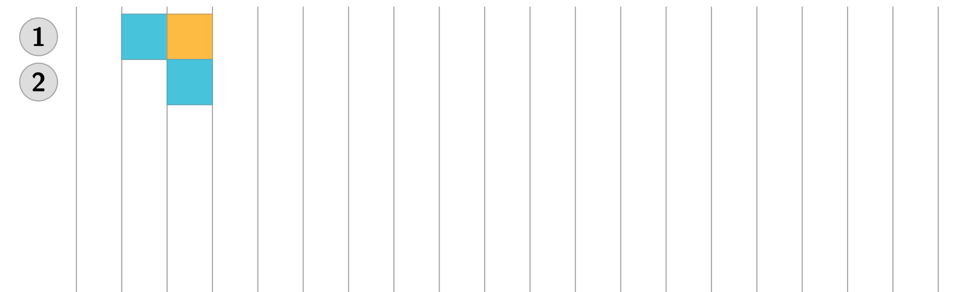
Instruction	FU	rd
1	LSU	x12



Scoreboard: Example

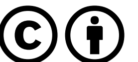
```
① ld x12, 8(x9)
② ld x13, 0(x7)
  mul x17, x13, x12
  subi x18, x12, 2
  mul x13, x12, x18
  add x10, x17, x13
```

Execution Diagram



0: #1 can be started
1: #2 can be started, #1 reads operands
2: #3 is blocked (hazards)

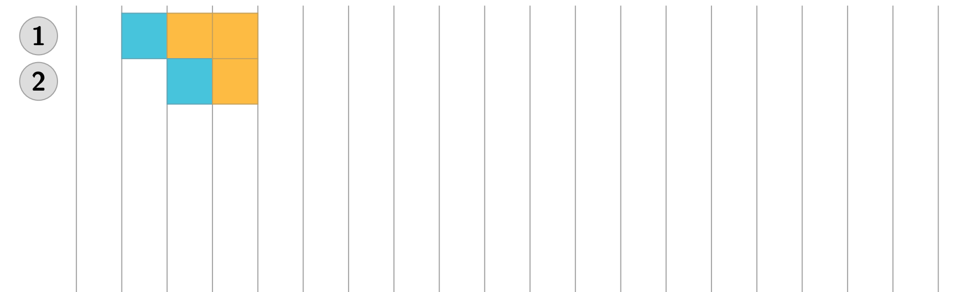
Instruction	FU	rd
1	LSU	x12
2	LSU	x13



Scoreboard: Example

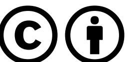
```
(1) ld x12, 8(x9)
(2) ld x13, 0(x7)
    mul x17, x13, x12
    subi x18, x12, 2
    mul x13, x12, x18
    add x10, x17, x13
```

Execution Diagram



0: #1 can be started
1: #2 can be started, #1 reads operands
2: #3 is blocked (hazards)
3: #1 will complete now

Instruction	FU	rd
1	LSU	x12
2	LSU	x13

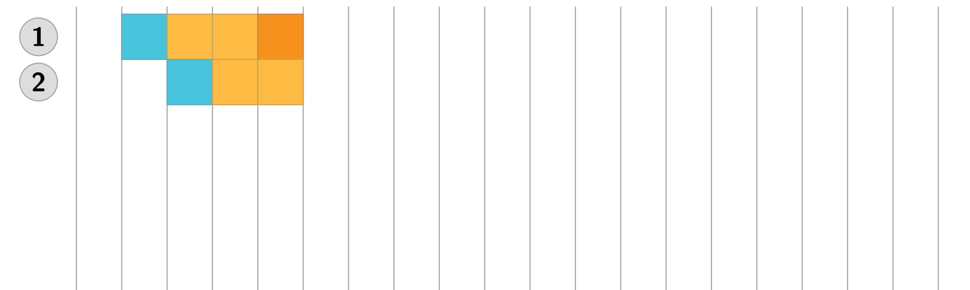


Scoreboard: Example

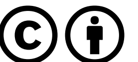
```
(1) ld x12, 8(x9)
(2) ld x13, 0(x7)
    mul x17, x13, x12
    subi x18, x12, 2
    mul x13, x12, x18
    add x10, x17, x13
```

Instruction	FU	rd
~~1~~	~~LSU~~	~~x12~~
2	LSU	x13

Execution Diagram



0: #1 can be started
1: #2 can be started, #1 reads operands
2: #3 is blocked (hazards)
3: #1 will complete now
4: #1 writes result, #2 will complete too

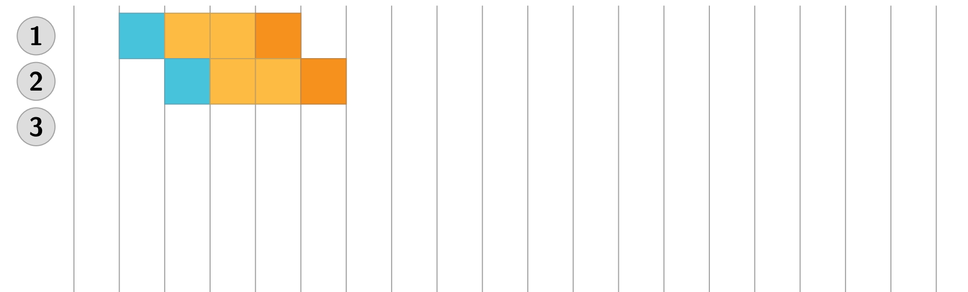


Scoreboard: Example

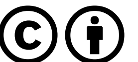
```
① ld x12, 8(x9)
② ld x13, 0(x7)
③ mul x17, x13, x12
  subi x18, x12, 2
  mul x13, x12, x18
  add x10, x17, x13
```

Instruction	FU	rd
~~②~~	~~LSU~~	~~x13~~

Execution Diagram



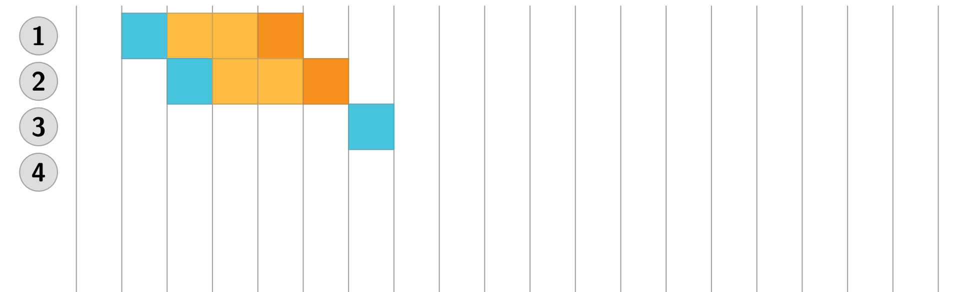
0: #1 can be started
1: #2 can be started, #1 reads operands
2: #3 is blocked (hazards)
3: #1 will complete now
4: #1 writes result, #2 will complete too
5: #2 in WB, #3 can be started



Scoreboard: Example

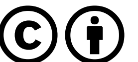
```
① ld x12, 8(x9)
② ld x13, 0(x7)
③ mul x17, x13, x12
④ subi x18, x12, 2
  mul x13, x12, x18
  add x10, x17, x13
```

Execution Diagram



0: #1 can be started
1: #2 can be started, #1 reads operands
2: #3 is blocked (hazards)
3: #1 will complete now
4: #1 writes result, #2 will complete too
5: #2 in WB, #3 can be started
6: #4 can be started

Instruction	FU	rd
③	MUL	x17



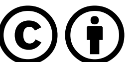
Scoreboard: Example

```
1 ld x12, 8(x9)
2 ld x13, 0(x7)
3 mul x17, x13, x12
4 subi x18, x12, 2
  mul x13, x12, x18
  add x10, x17, x13
```

Instruction	FU	rd
3	MUL	x17
4	ALU	x18

Execution Diagram

0: #1 can be started
1: #2 can be started, #1 reads operands
2: #3 is blocked (hazards)
3: #1 will complete now
4: #1 writes result, #2 will complete too
5: #2 in WB, #3 can be started
6: #4 can be started
7: #5 blocked



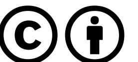
Scoreboard: Example

```
① ld x12, 8(x9)
② ld x13, 0(x7)
③ mul x17, x13, x12
④ subi x18, x12, 2
  mul x13, x12, x18
  add x10, x17, x13
```

Execution Diagram

0: #1 can be started
1: #2 can be started, #1 reads operands
2: #3 is blocked (hazards)
3: #1 will complete now
4: #1 writes result, #2 will complete too
5: #2 in WB, #3 can be started
6: #4 can be started
7: #5 blocked

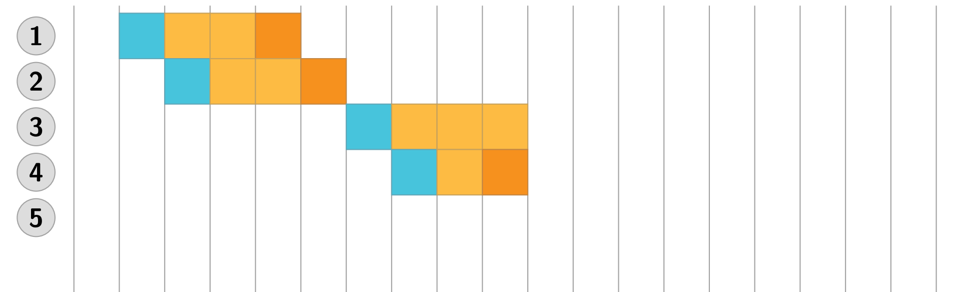
Instruction	FU	rd
3	MUL	x17
4	ALU	x18



Scoreboard: Example

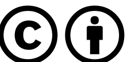
```
1 ld x12, 8(x9)
2 ld x13, 0(x7)
3 mul x17, x13, x12
4 subi x18, x12, 2
5 mul x13, x12, x18
  add x10, x17, x13
```

Execution Diagram



0: #1 can be started
1: #2 can be started, #1 reads operands
2: #3 is blocked (hazards)
3: #1 will complete now
4: #1 writes result, #2 will complete too
5: #2 in WB, #3 can be started
6: #4 can be started
7: #5 blocked
9: #4 in WB, #5 can be started

Instruction	FU	rd
3	MUL	x17
~~4~~	~~ALU~~	~~x18~~

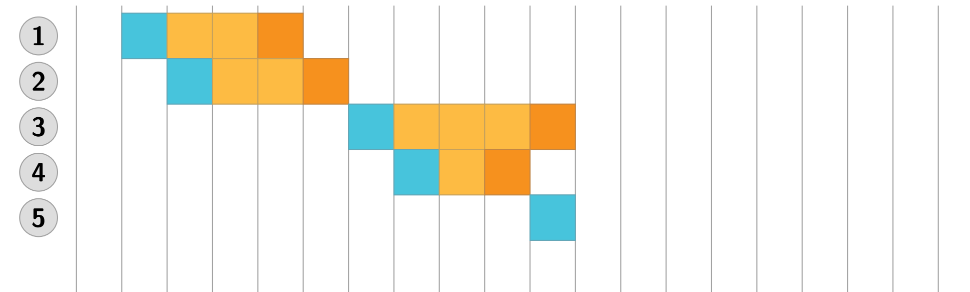


Scoreboard: Example

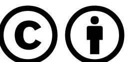
```
① ld x12, 8(x9)
② ld x13, 0(x7)
③ mul x17, x13, x12
④ subi x18, x12, 2
⑤ mul x13, x12, x18
  add x10, x17, x13
```

Instruction	FU	rd
~~3~~	~~MUL~~	~~x17~~
5	MUL	x13

Execution Diagram



0: #1 can be started
1: #2 can be started, #1 reads operands
2: #3 is blocked (hazards)
3: #1 will complete now
4: #1 writes result, #2 will complete too
5: #2 in WB, #3 can be started
6: #4 can be started
7: #5 blocked
9: #4 in WB, #5 can be started
10: #6 is blocked

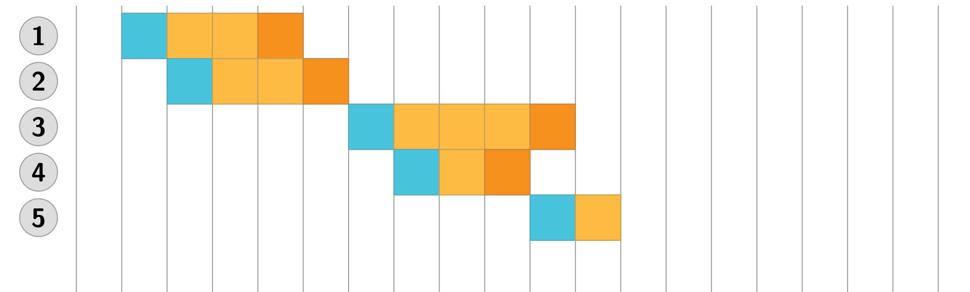


Scoreboard: Example

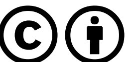
```
① ld x12, 8(x9)
② ld x13, 0(x7)
③ mul x17, x13, x12
④ subi x18, x12, 2
⑤ mul x13, x12, x18
  add x10, x17, x13
```

Instruction	FU	rd
⑤	MUL	x13

Execution Diagram



0: #1 can be started
1: #2 can be started, #1 reads operands
2: #3 is blocked (hazards)
3: #1 will complete now
4: #1 writes result, #2 will complete too
5: #2 in WB, #3 can be started
6: #4 can be started
7: #5 blocked
9: #4 in WB, #5 can be started
10: #6 is blocked

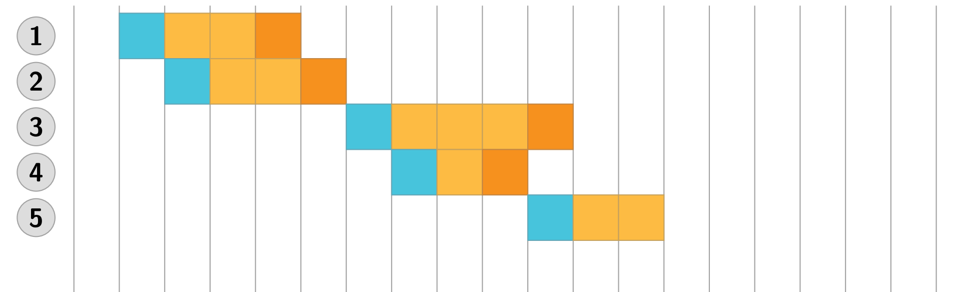


Scoreboard: Example

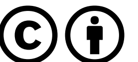
```
① ld x12, 8(x9)
② ld x13, 0(x7)
③ mul x17, x13, x12
④ subi x18, x12, 2
⑤ mul x13, x12, x18
  add x10, x17, x13
```

Instruction	FU	rd
⑤	MUL	x13

Execution Diagram



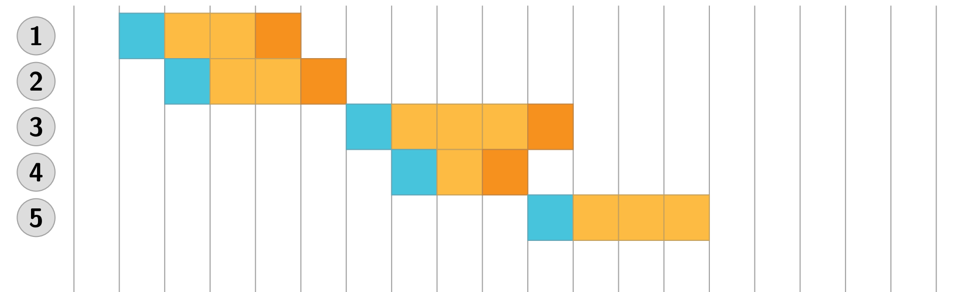
0: #1 can be started
1: #2 can be started, #1 reads operands
2: #3 is blocked (hazards)
3: #1 will complete now
4: #1 writes result, #2 will complete too
5: #2 in WB, #3 can be started
6: #4 can be started
7: #5 blocked
9: #4 in WB, #5 can be started
10: #6 is blocked



Scoreboard: Example

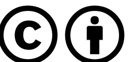
```
① ld x12, 8(x9)
② ld x13, 0(x7)
③ mul x17, x13, x12
④ subi x18, x12, 2
⑤ mul x13, x12, x18
  add x10, x17, x13
```

Execution Diagram



0: #1 can be started
1: #2 can be started, #1 reads operands
2: #3 is blocked (hazards)
3: #1 will complete now
4: #1 writes result, #2 will complete too
5: #2 in WB, #3 can be started
6: #4 can be started
7: #5 blocked
9: #4 in WB, #5 can be started
10: #6 is blocked

Instruction	FU	rd
5	MUL	x13

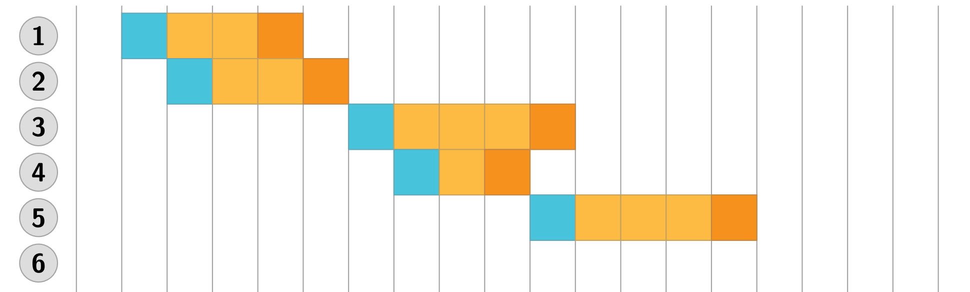


Scoreboard: Example

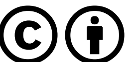
```
1 ld x12, 8(x9)
2 ld x13, 0(x7)
3 mul x17, x13, x12
4 subi x18, x12, 2
5 mul x13, x12, x18
6 add x10, x17, x13
```

Instruction	FU	rd
~~5~~	~~MUL~~	~~x13~~

Execution Diagram



0: #1 can be started
1: #2 can be started, #1 reads operands
2: #3 is blocked (hazards)
3: #1 will complete now
4: #1 writes result, #2 will complete too
5: #2 in WB, #3 can be started
6: #4 can be started
7: #5 blocked
9: #4 in WB, #5 can be started
10: #6 is blocked
14: #5 in WB, #6 can be started

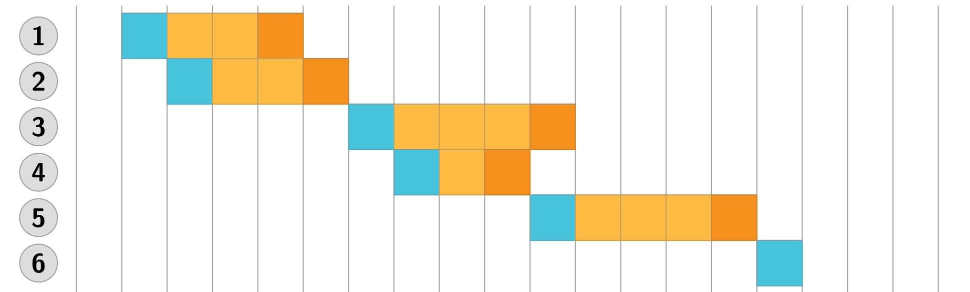


Scoreboard: Example

```
1 ld x12, 8(x9)
2 ld x13, 0(x7)
3 mul x17, x13, x12
4 subi x18, x12, 2
5 mul x13, x12, x18
6 add x10, x17, x13
```

Instruction	FU	rd
6	ALU	x10

Execution Diagram



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1: #2 can be started, #1 reads operands
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3: #1 will complete now
4: #1 writes result, #2 will complete too
5: #2 in WB, #3 can be started
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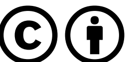
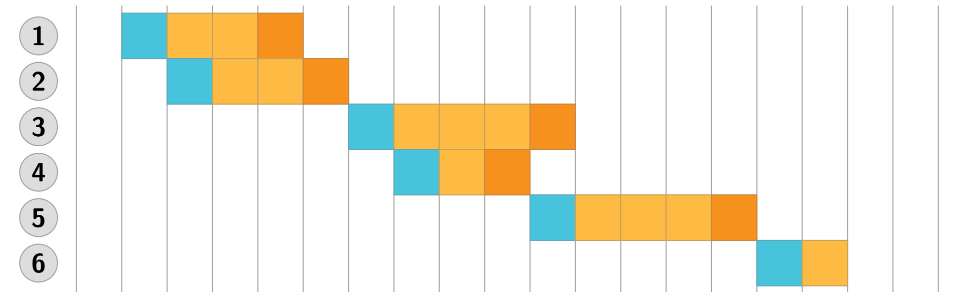
7: #5 blocked
9: #4 in WB, #5 can be started
10: #6 is blocked
14: #5 in WB, #6 can be started



Scoreboard: Example

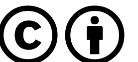
```
① ld x12, 8(x9)
② ld x13, 0(x7)
③ mul x17, x13, x12
④ subi x18, x12, 2
⑤ mul x13, x12, x18
⑥ add x10, x17, x13
```

Execution Diagram



Instruction	FU	rd
6	ALU	x10

0: #1 can be started
1: #2 can be started, #1 reads operands
2: #3 is blocked (hazards)
3: #1 will complete now
4: #1 writes result, #2 will complete too
5: #2 in WB, #3 can be started
6: #4 can be started
7: #5 blocked
9: #4 in WB, #5 can be started
10: #6 is blocked
14: #5 in WB, #6 can be started

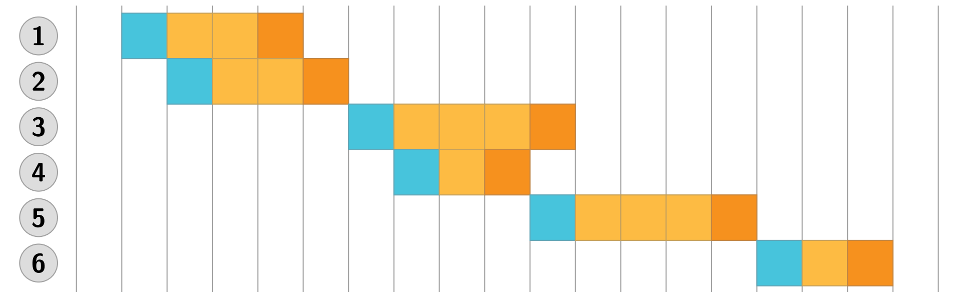


Scoreboard: Example

```
1 ld x12, 8(x9)
2 ld x13, 0(x7)
3 mul x17, x13, x12
4 subi x18, x12, 2
5 mul x13, x12, x18
6 add x10, x17, x13
```

Instruction	FU	rd
~~6~~	~~ALU~~	~~x10~~

Execution Diagram



0: #1 can be started
1: #2 can be started, #1 reads operands
2: #3 is blocked (hazards)
3: #1 will complete now
4: #1 writes result, #2 will complete too
5: #2 in WB, #3 can be started
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9: #4 in WB, #5 can be started
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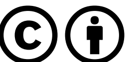
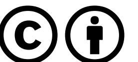


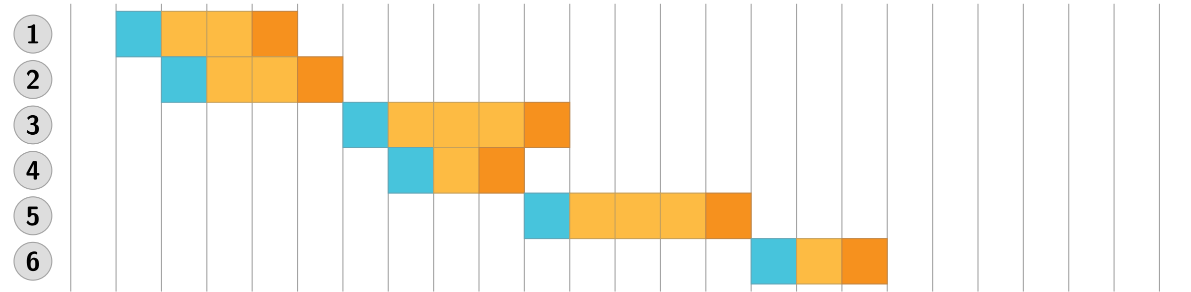
Example: Ariane CPU

https://github.com/pulp-platform/ariane/



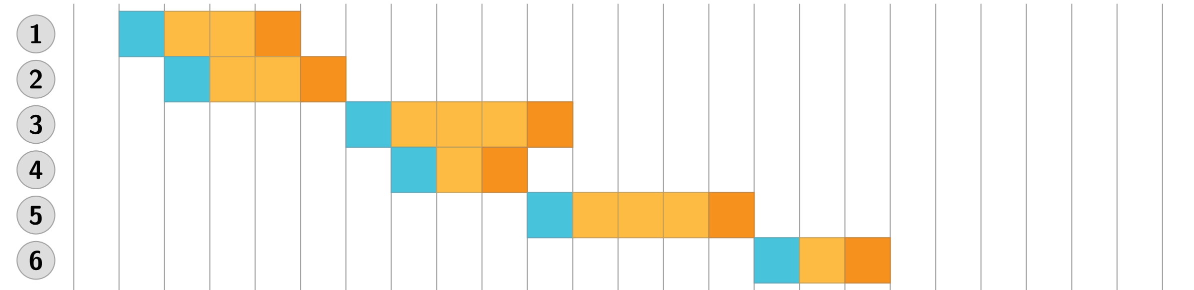
Limits of In-Order Issue

```
1 ld x12, 8(x9)
2 ld x13, 0(x7)
3 mul x17, x13, x12
4 subi x18, x12, 2
5 mul x13, x12, x18
6 add x10, x17, x13
```

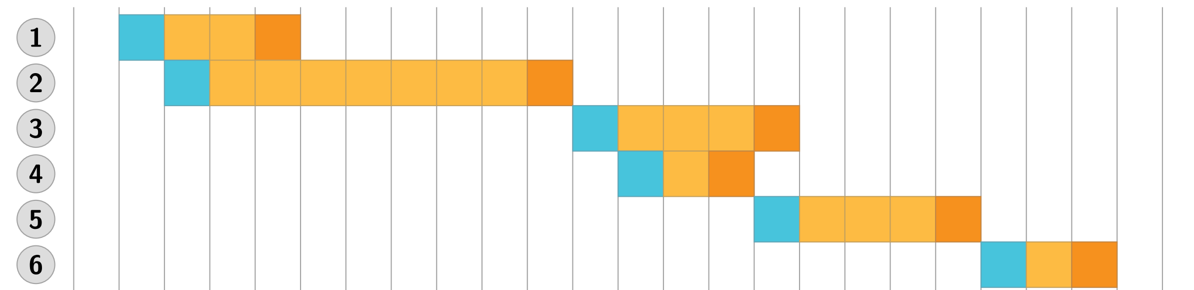


Limits of In-Order Issue

```
① ld x12, 8(x9)
② ld x13, 0(x7)
③ mul x17, x13, x12
④ subi x18, x12, 2
⑤ mul x13, x12, x18
⑥ add x10, x17, x13
```



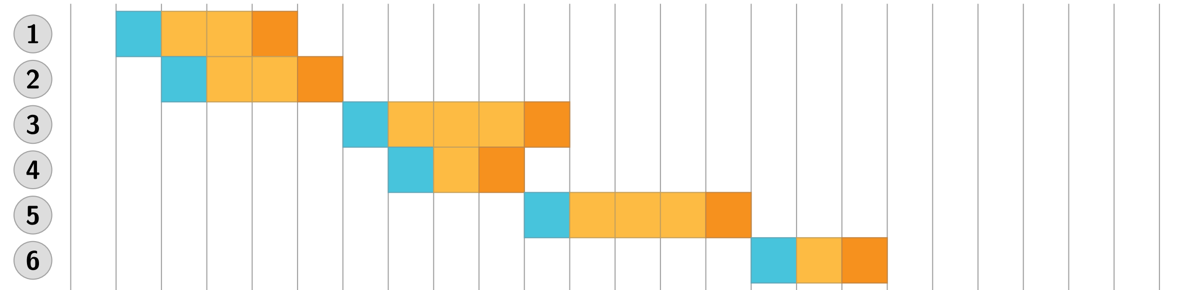
Delayed Load Instruction



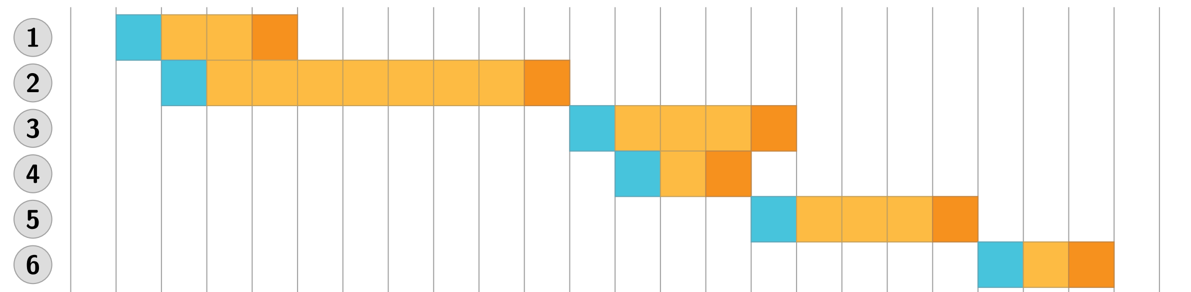
CC BY

Limits of In-Order Issue

```
1 ld x12, 8(x9)
2 ld x13, 0(x7)
3 mul x17, x13, x12
4 subi x18, x12, 2
5 mul x13, x12, x18
6 add x10, x17, x13
```



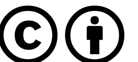
Delayed Load Instruction



Recap: data flow model, approach: reorder instructions

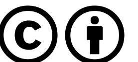
(c)(i)

Out-of-Order Issue



Out-of-Order Issue

Start of instructions in arbitrary order



Out-of-Order Issue

Start of instructions in arbitrary order

- As soon as hazards of each instruction are resolved

Out-of-Order Issue

Start of instructions in arbitrary order

- As soon as hazards of each instruction are resolved
- Instruction buffer has window of next N instructions

Out-of-Order Issue

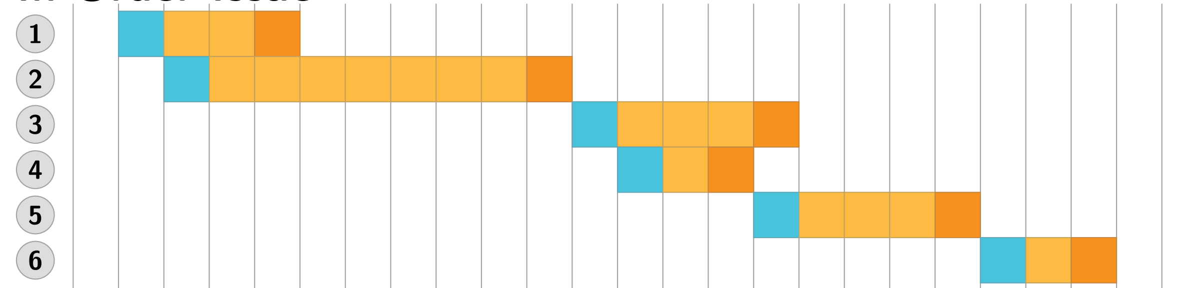
Start of instructions in arbitrary order

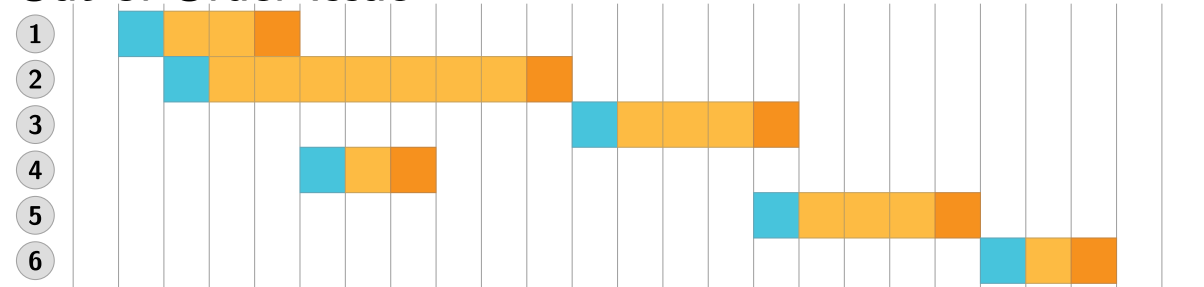
- As soon as hazards of each instruction are resolved
- Instruction buffer has window of next N instructions

But: Out-of-order issue does not improve very much alone!

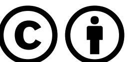
Out-of-Order: Example

```
1 ld x12, 8(x9)
2 ld x13, 0(x7)
3 mul x17, x13, x12
4 subi x18, x12, 2
5 mul x13, x12, x18
6 add x10, x17, x13
```



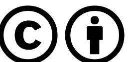


Out-of-Order Limits



Out-of-Order Limits

WAW and WAR limit further reordering



Out-of-Order Limits

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WAW and WAR limit further reordering

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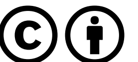

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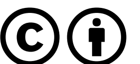
- Number of registers limited by ISA



Out-of-Order Limits

WAW and WAR limit further reordering

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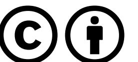

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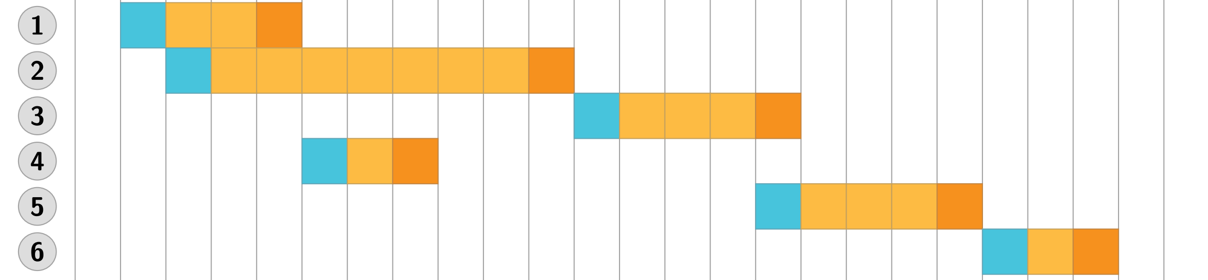
- Number of registers limited by ISA
- Compiler optimizations limited
- Especially with different execution paths

Approach: CPU solves problem by register renaming

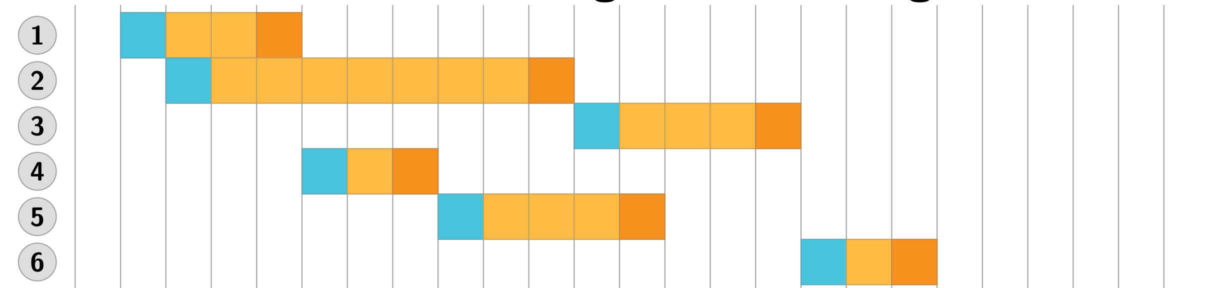
Register Renaming: Example

```
1 ld x12, 8(x9)
2 ld x13, 0(x7)
3 mul x17, x13, x12
4 subi x18, x12, 2
5 mul x13, x12, x18
6 add x10, x17, x13
```

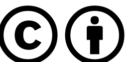
Out-of-Order Issue



Out-of-Order Issue with Register Renaming

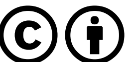


Register Renaming



Register Renaming

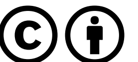
Approach: Use microarchitecture ("virtual" register names)



Register Renaming

Approach: Use microarchitecture (”virtual” register names)

- Entirely eliminates WAR and WAW hazards



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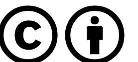

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- Format of reservation stations (multiple entries per FU)
  - Op: Operation
  - Qj, Qk: Reservation station that produces source registers (pending)

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  - Op: Operation
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  - Op: Operation
  - Qj, Qk: Reservation station that produces source registers (pending)
  - Vj, Vk: Value of source register (once available)
  - Busy: Reservation station is active
- Additionally: Register result status shows which RS produces registers

Tomasulo: Example

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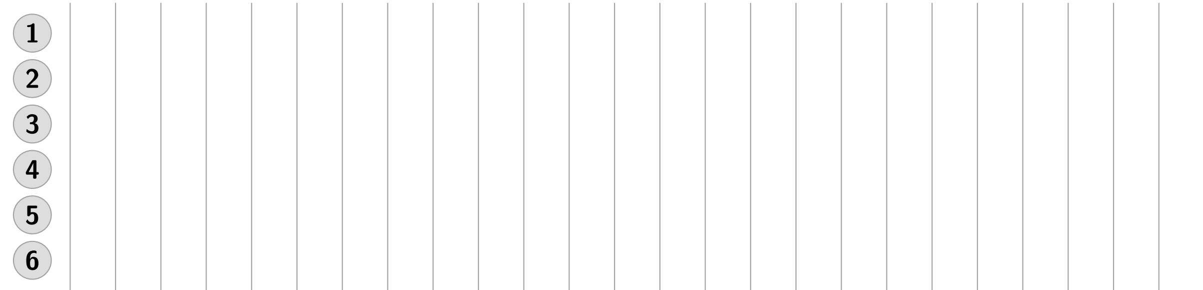
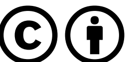
```



	ALU					LSU					MUL				
	Insn	Vj	Vk	Qj	Qk	Insn	Vj	Vk	Qj	Qk	Insn	Vj	Vk	Qj	Qk
0															
1															



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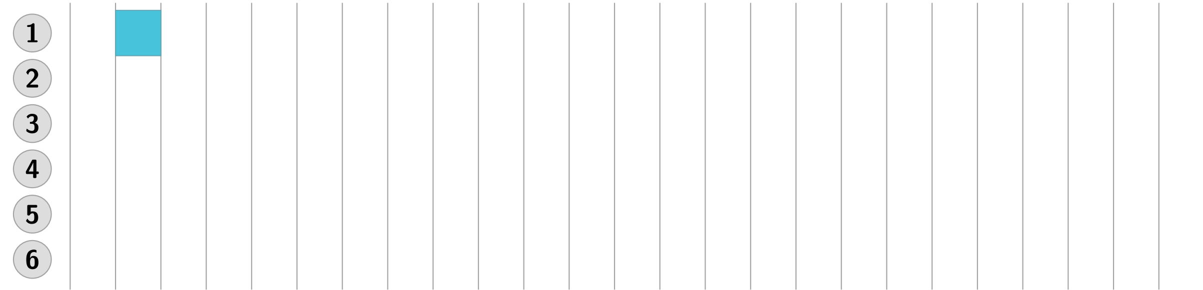
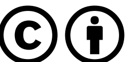


	ALU					LSU					MUL				
	Insn	Vj	Vk	Qj	Qk	Insn	Vj	Vk	Qj	Qk	Insn	Vj	Vk	Qj	Qk
0						1	8	...	-	-					
1															



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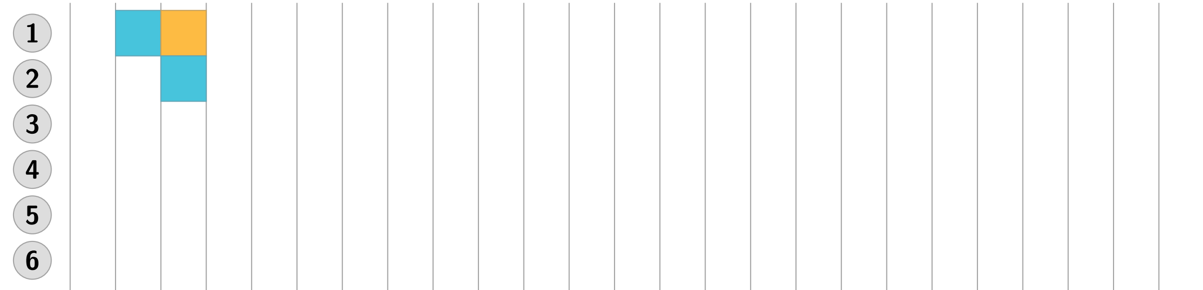

	ALU					LSU					MUL				
	Insn	Vj	Vk	Qj	Qk	Insn	Vj	Vk	Qj	Qk	Insn	Vj	Vk	Qj	Qk
0						1	8	...	-	-					
1						2	0	...	-	-					

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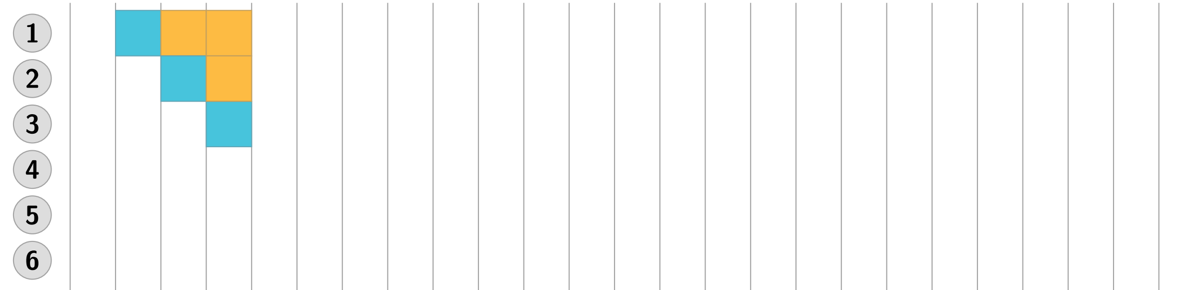

	ALU					LSU					MUL				
	Insn	Vj	Vk	Qj	Qk	Insn	Vj	Vk	Qj	Qk	Insn	Vj	Vk	Qj	Qk
0						1	8	...	-	-	3	-	-	LSU0	LSU1
1						2	0	...	-	-					

Prof. Dr.-Ing. Stefan Wallentowitz – Department 07 – Munich University of Applied Sciences

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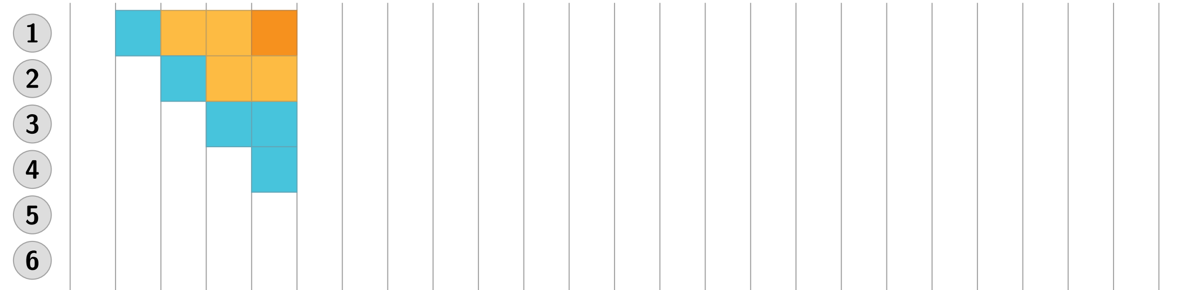

	ALU					LSU					MUL				
	Insn	Vj	Vk	Qj	Qk	Insn	Vj	Vk	Qj	Qk	Insn	Vj	Vk	Qj	Qk
0	4	-	2	LSU0	-	1	8	...	-	-	3	-	-	LSU0	LSU1
1						2	0	...	-	-					

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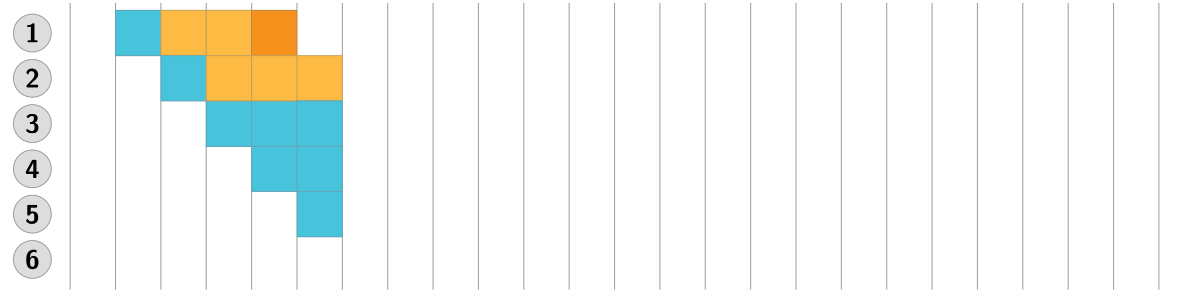

	ALU					LSU					MUL				
	Insn	Vj	Vk	Qj	Qk	Insn	Vj	Vk	Qj	Qk	Insn	Vj	Vk	Qj	Qk
0	4	...	2	~~LSU0~~	-	~~1~~	~~8~~	~~...~~	-	-	3	...	-	~~LSU0~~	LSU1
1						2	0	...	-	-	5	...	-	-	ALU0

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Tomasulo: Example

```
① ld x12, 8(x9)
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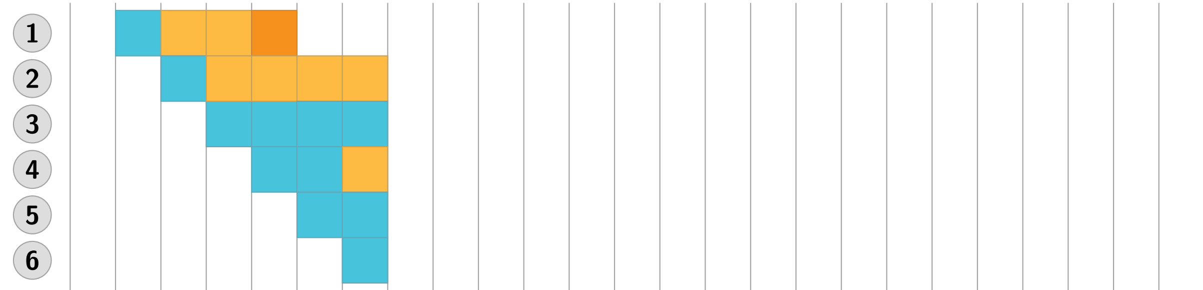
```



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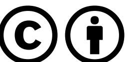
	Insn	Vj	Vk	Qj	Qk	Insn	Vj	Vk	Qj	Qk	Insn	Vj	Vk	Qj	Qk
0	4	...	2	-	-						3	...	-	-	LSU1
1	6	-	-	MUL0	MUL1	2	0	...	-	-	5	...	-	-	ALU0



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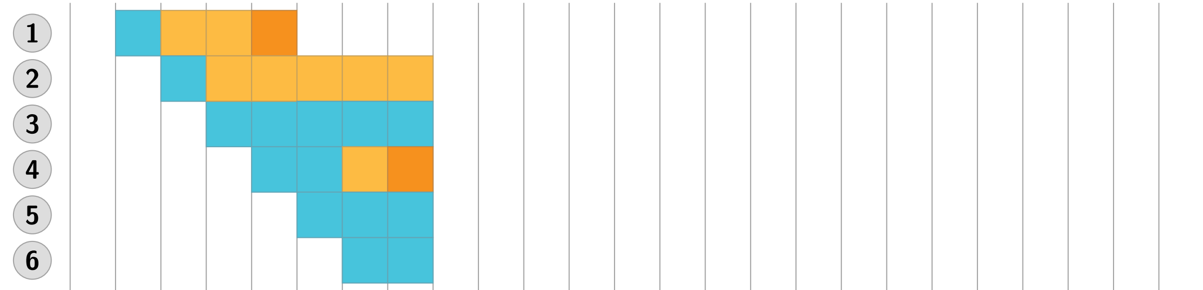

	ALU					LSU					MUL				
	Insn	Vj	Vk	Qj	Qk	Insn	Vj	Vk	Qj	Qk	Insn	Vj	Vk	Qj	Qk
0	4	...	2	-	-						3	...	-	-	LSU1
1	6	-	-	MUL0	MUL1	2	0	...	-	-	5	...	-	-	ALU0

(c)(i)

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	Insn	Vj	Vk	Qj	Qk	Insn	Vj	Vk	Qj	Qk	Insn	Vj	Vk	Qj	Qk
0	4	~~...~~	~~2~~	-	-						3	...	-	-	LSU1
1	6	-	-	MUL0	MUL1	2	0	...	-	-	5	...	...	-	~~ALU0~~

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① ld x12, 8(x9)
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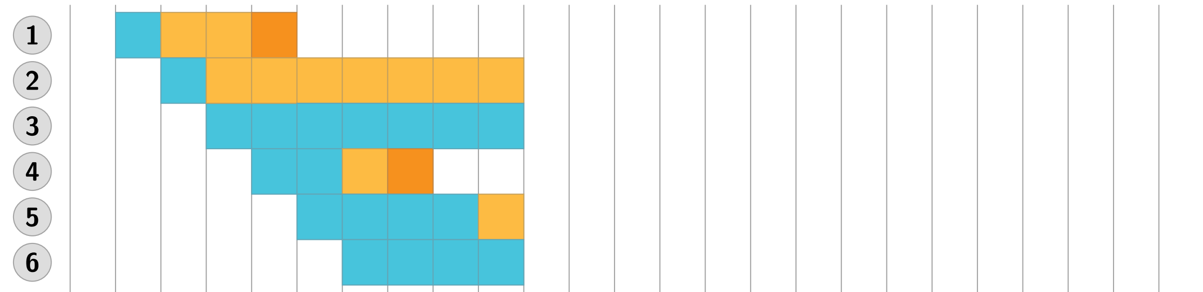

	ALU					LSU					MUL				
	Insn	Vj	Vk	Qj	Qk	Insn	Vj	Vk	Qj	Qk	Insn	Vj	Vk	Qj	Qk
0											3	...	-	-	LSU1
1	6	-	-	MUL0	MUL1	2	0	...	-	-	5	...	...	-	-

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```
① ld x12, 8(x9)
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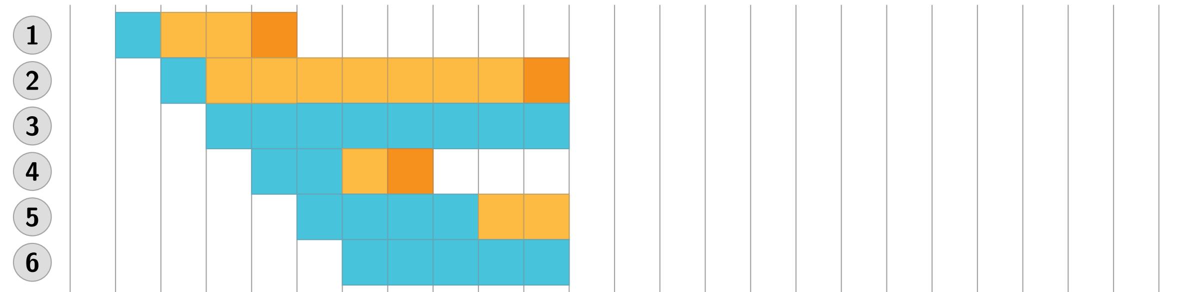

	ALU					LSU					MUL				
	Insn	Vj	Vk	Qj	Qk	Insn	Vj	Vk	Qj	Qk	Insn	Vj	Vk	Qj	Qk
0											3	...	-	-	LSU1
1	6	-	-	MUL0	MUL1	2	0	...	-	-	5	...	...	-	-

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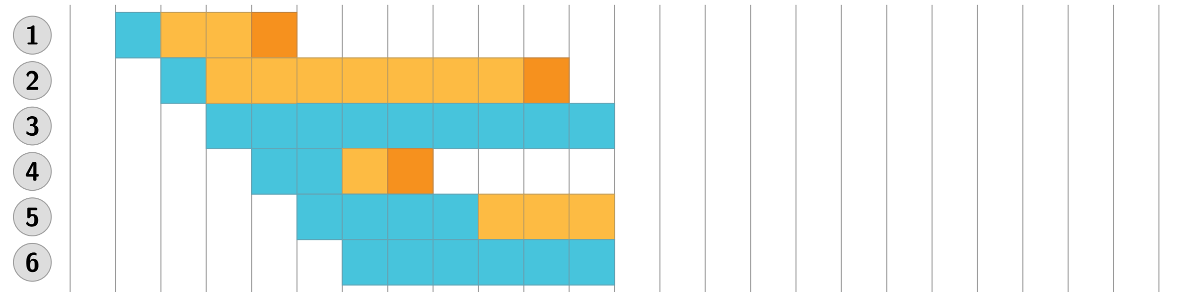

	ALU					LSU					MUL				
	Insn	Vj	Vk	Qj	Qk	Insn	Vj	Vk	Qj	Qk	Insn	Vj	Vk	Qj	Qk
0											3	…	…	-	~~LSU1~~
1	6	-	-	MUL0	MUL1	~~2~~	~~0~~	~~…~~	-	-	5	…	…	-	-

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① ld x12, 8(x9)
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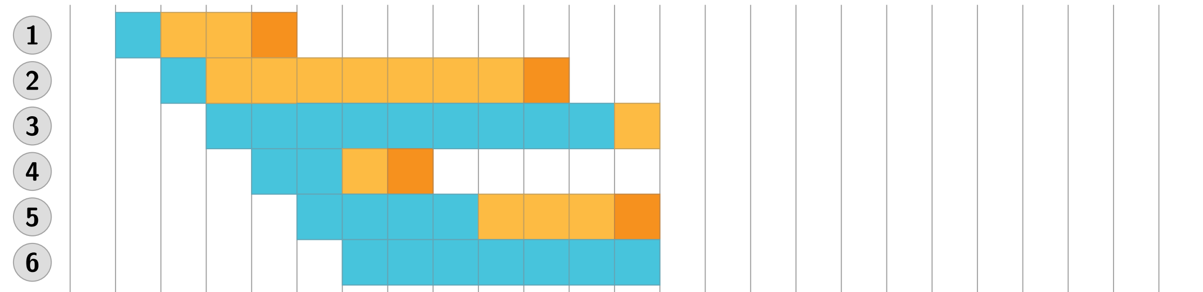
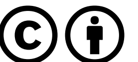


	ALU					LSU					MUL				
	Insn	Vj	Vk	Qj	Qk	Insn	Vj	Vk	Qj	Qk	Insn	Vj	Vk	Qj	Qk
0											3	...	...	-	-
1	6	-	-	MUL0	MUL1						5	...	...	-	-



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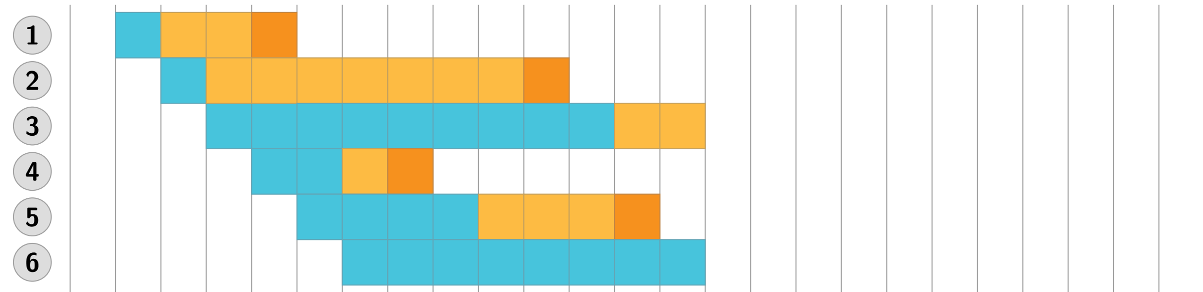

	ALU					LSU					MUL				
	Insn	Vj	Vk	Qj	Qk	Insn	Vj	Vk	Qj	Qk	Insn	Vj	Vk	Qj	Qk
0											3	...	...	-	-
1	6	-	...	MUL0	~~MUL1~~						~~5~~	~~...~~	~~...~~	-	-

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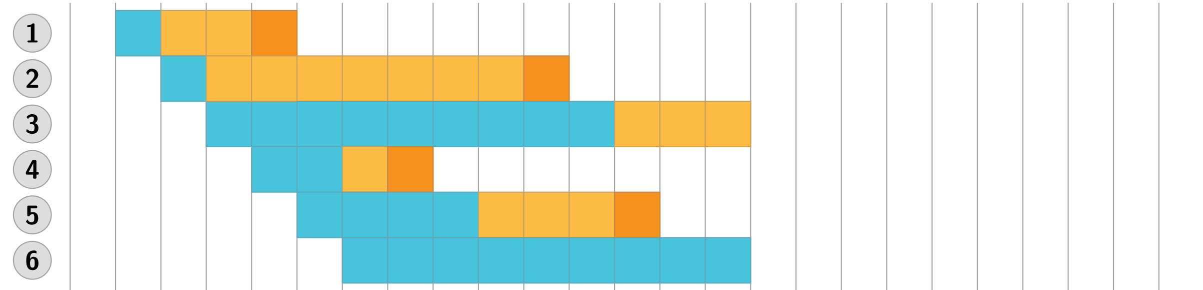

	ALU					LSU					MUL				
	Insn	Vj	Vk	Qj	Qk	Insn	Vj	Vk	Qj	Qk	Insn	Vj	Vk	Qj	Qk
0											3	...	...	-	-
1	6	-	...	MUL0											

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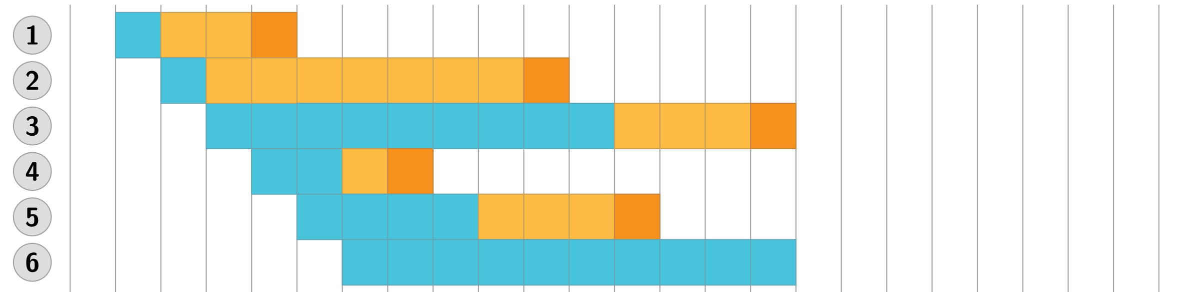
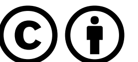


	ALU					LSU					MUL				
	Insn	Vj	Vk	Qj	Qk	Insn	Vj	Vk	Qj	Qk	Insn	Vj	Vk	Qj	Qk
0											3	...	...	-	-
1	6	-	...	MUL0											



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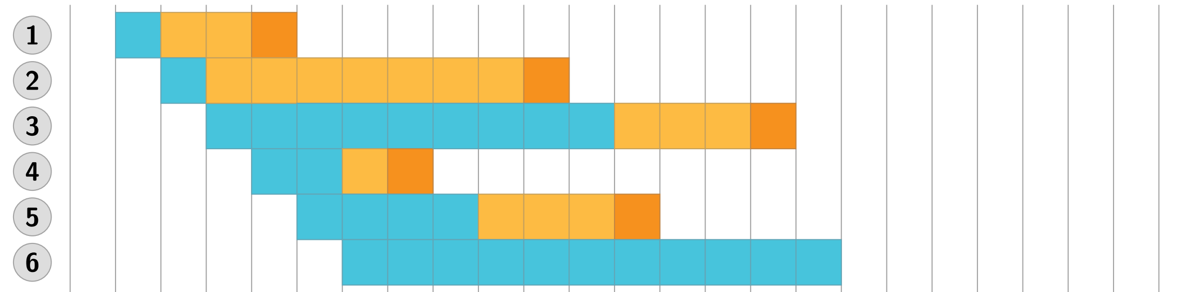
2 ld x13, 0(x7)
3 mul x17, x13, x12
4 subi x18, x12, 2
5 mul x13, x12, x18
6 add x10, x17, x13
```



	ALU					LSU					MUL				
	Insn	Vj	Vk	Qj	Qk	Insn	Vj	Vk	Qj	Qk	Insn	Vj	Vk	Qj	Qk
0											~~3~~	~~...~~	~~...~~	-	-
1	6	...	...	~~MUL0~~											

CC BY

Tomasulo: Example

```
① ld x12, 8(x9)
② ld x13, 0(x7)
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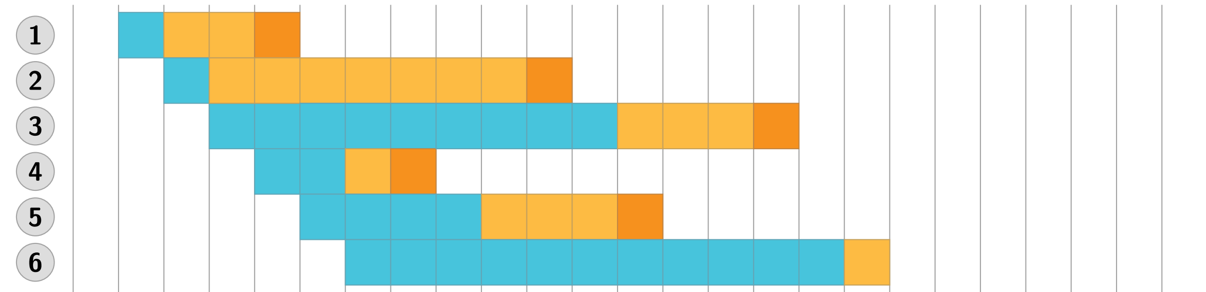

	ALU					LSU					MUL				
	Insn	Vj	Vk	Qj	Qk	Insn	Vj	Vk	Qj	Qk	Insn	Vj	Vk	Qj	Qk
0															
1	6	…	…												

(c)(i)

Tomasulo: Example

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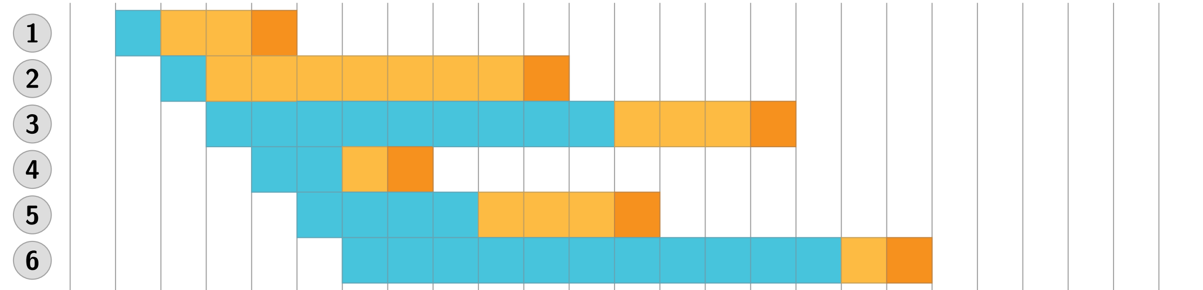

	ALU					LSU					MUL				
	Insn	Vj	Vk	Qj	Qk	Insn	Vj	Vk	Qj	Qk	Insn	Vj	Vk	Qj	Qk
0															
1	6	…	…												

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Tomasulo: Example

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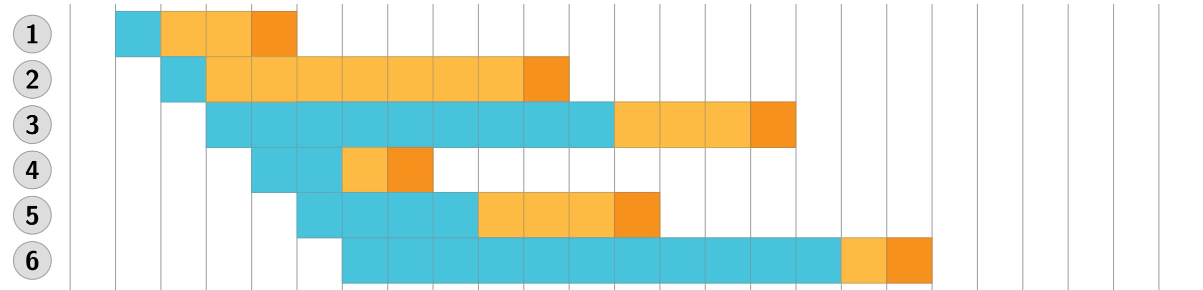

	ALU					LSU					MUL				
	Insn	Vj	Vk	Qj	Qk	Insn	Vj	Vk	Qj	Qk	Insn	Vj	Vk	Qj	Qk
0															
1	~~6~~	...	...												

(c)(i)